Understanding Constraints

Constraint files are simple documents within the system and can be compiled to add more intelligence to the whole process.

A constraint document contains a list of statements, known as constraint groups, each of which targets one or more objects and contains one or more constraints.

The following example constraint group, shown in the typical constraint group syntax, specifies the target FPGA device:

```
Record=Constraint | TargetKind=Part | TargetId=XC2S300E-6PQ208C
```

Each constraint group can include multiple constraints, for example a constraint group can be added that targets a bus (a collection of nets). Multiple constraints can then be added to target the individual items within the bus. The file syntax of this would be:

```
Record=Constraint | TargetKind=Port | TargetId=DB[7..0] |
FPGA_PINNUM=P8,P7,P6,P5,P4,P3,P206,P205 |
FPGA_SLEW=FAST,FAST,FAST,FAST,FAST,FAST,FAST,FAST
```

This example specifies a set of constraints that target the Ports DB7..DB0. It then supplies eight FPGA_PINNUM constraints and eight FPGA_SLEW constraints.

Note that bus ports can be described in a constraint and then later, after compiling, these can be mapped to individual pins. There is no need to specify both levels (bus and single) as separate constraints.

Multiple constraints can target the same Port. For example the following constraint groups target the port CLK_REF; the first specifies the pin number, the second specifies that this pin must be configured as a clock pin, the third specifies that this net must use a global clock resource, the forth specifies that the place and route process should attempt to route this to achieve the specified frequency.

```
Record=Constraint | TargetKind=Port | TargetId=CLK_REF | FPGA_PINNUM=P185

Record=Constraint | TargetKind=Port | TargetId=CLK_REF | FPGA_CLOCK_PIN=TRUE

Record=Constraint | TargetKind=Port | TargetId=CLK_REF | FPGA_CLOCK=TRUE

Record=Constraint | TargetKind=Port | TargetId=CLK_REF | FPGA_CLOCK_FREQUENCY=50 Mhz
```

Alternatively, these constraint requirements could be specified in the one constraint group:

```
Record=Constraint | TargetKind=Port | TargetId=CLK_REF | FPGA_PINNUM=P185 |
FPGA_CLOCK_PIN=TRUE | FPGA_CLOCK=TRUE | FPGA_CLOCK_FREQUENCY=50 Mhz
```

A more appropriate way to group them would be a group of those that are design-type information, and another for those that are device-on-PCB type information, in separate constraint files. For example, the design-type constraint file would include:

```
Record=Constraint | TargetKind=Port | TargetId=CLK_REF | FPGA_CLOCK=TRUE

Record=Constraint | TargetKind=Port | TargetId=CLK_REF | FPGA_CLOCK_FREQUENCY=50 Mhz
```

And the device-on-PCB type constraint file would include:

```
Record=Constraint | TargetKind=Port | TargetId=CLK_REF | FPGA_PINNUM=P185

Record=Constraint | TargetKind=Port | TargetId=CLK_REF | FPGA_CLOCK_PIN=TRUE
```

Note that they have been kept as separate entries in the constraint files for readability.

See Also

For more information on supported constraints, see Constraint File Reference.

For information on the constraint system in place for the Desktop NanoBoard, see Understanding the Desktop NanoBoard NB2DSK01 Constraint System.