

# CAM Editor Data Verification

Contents

- Import the Data
  - Creating a new CAM Document
  - Importing Files Using Quick Load
- Verify Layer Assignments
- Verify Layers Order
- Verify Layers Sets
- Extract and Rename the Netlist
  - Renaming Nets
- Run Design Rules Check
  - Setting Up the DRC
  - Querying a Violation for Further Information
- Using Auto Fix
  - Using Auto Fix in the CAM Panel
  - Checking Remaining Violations

# ***Altium***



This tutorial follows the steps that must be taken in order to extract a valid netlist from imported Gerber, NC Drill or ODB++ files, run a design rule check (DRC) on that data in Altium Designer's CAM Editor (CAMtastic®) and verify or modify the data.

Altium Designer's CAM Editor allows you to import Gerber and NC drill files and then run a set of design rules to verify the data in the imported files. Once verified, there is an Auto Fix option for many of these rules. The example Gerbers we will use in this tutorial have been generated from a PCB design named *4 Port Serial Interface* . All files necessary for this tutorial are supplied in the *Examples* folders of your Altium Designer installation.

## Import the Data

If your board has any holes, e.g. through holes or blind or buried vias, you must provide at least the signal layers (e.g. Gerber files for top and bottom) and one or more NC Drill file (Excellon 2 format). First, we will create a blank CAM file and then import the necessary files.

**For more information about setting up importing options, refer to the [CAM Editor Imports & Exports](#) tutorial.**

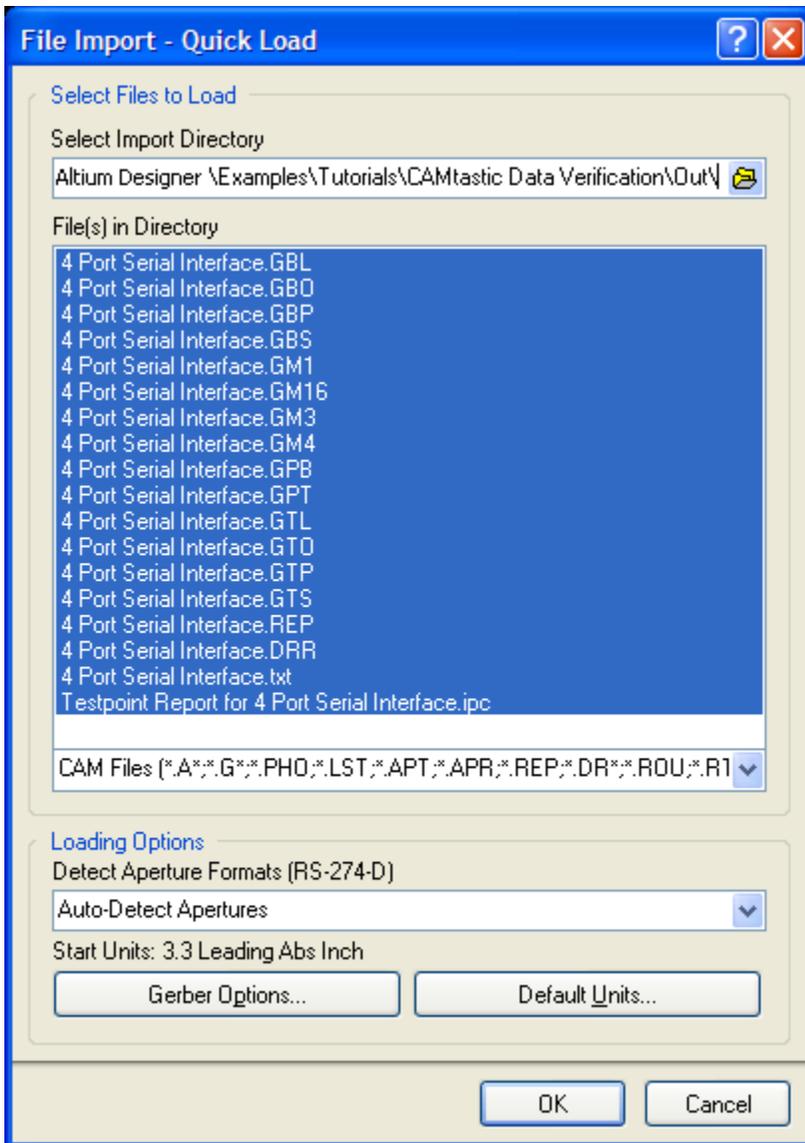
## Creating a new CAM Document

1. Create a new CAM document by selecting **File » New » CAM Document** from the menu. A new, blank CAM document, *CAM1.Cam* , appears in the design window.
2. Save the document by selecting **File » Save** (shortcut: **CTRL + S**). Type in a name, for example, *4 Port Serial.Cam*, browse to the location for your new CAM file and click **OK** .

## Importing Files Using Quick Load

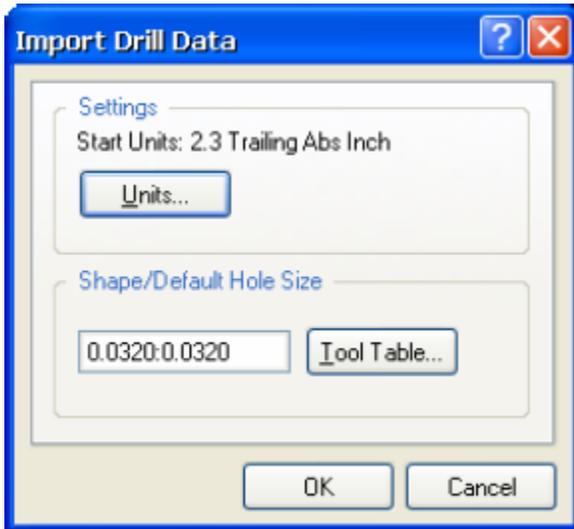
We are now ready to import the Gerber, NC Drill and netlist files into the new CAM document using the Quick Load option that imports all files found in the selected folder in one go.

1. Select **File » Import » Quick Load**. The *File Import - Quick Load* dialog displays.



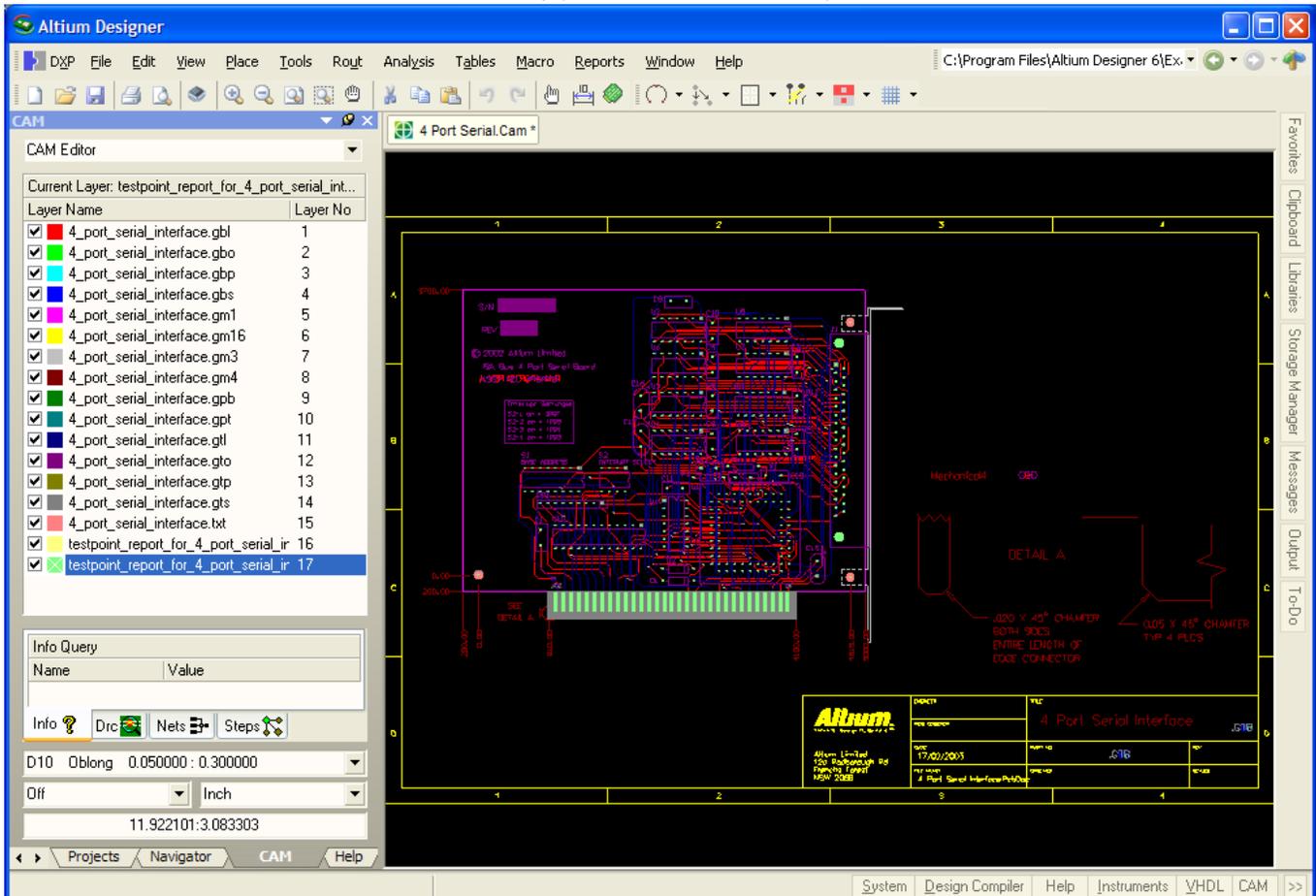
2. Click  to open the *Browse For Folder* dialog and navigate to the *CAM Data Verification\Out* folder of your Altium Designer installation. Click **OK**.

3. You will see a list of files found for importing in the chosen directory. Click **OK** to import the files and close the *File Import - Quick Load* dialog. The *Import Drill Data* dialog then opens.



4. Click **OK** to accept the default settings in the *Import Drill Data* dialog. The files are imported into the CAM Editor and display in the design window. A Quick Load Process Report is also generated.

5. Click the **CAM** button at the bottom of the workspace to open the **CAM** panel, where you can view the layer names and other information. Press **F1** over any panel to access the help.



6. Save the file (shortcut: **CTRL+ S**).

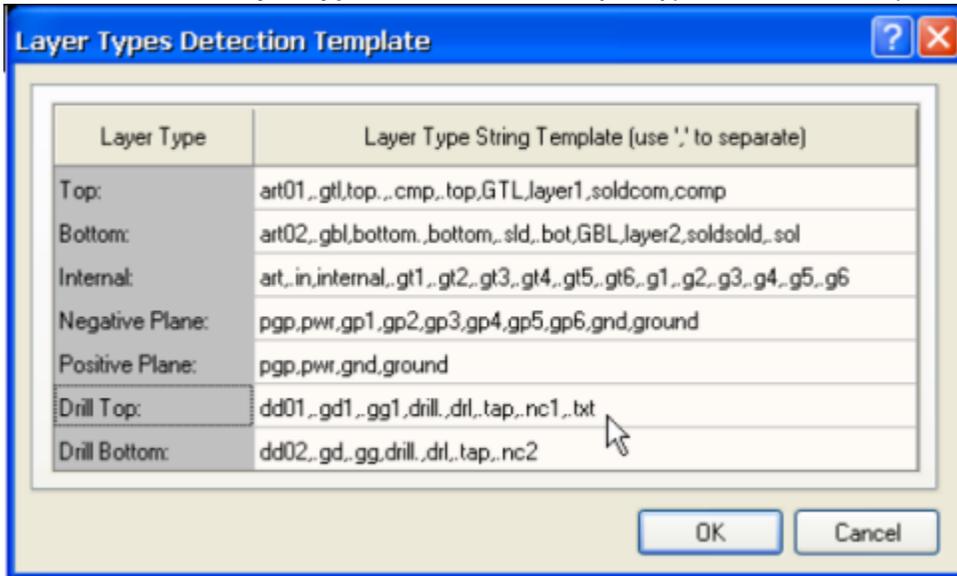
## Verify Layer Assignments

All Gerber, NC Drill and netlist layers in the CAM document must be assigned to an appropriate layer type.

The CAM Editor attempts to do this for you, matching the extensions of your Gerber files with those listed in the Layer Types Detection Template, but you should always review the Layers Table for completeness and accuracy. In this tutorial, we do not need to assign any layer type detection.

To view or modify the Layer Types Detection Template:

1. Select **Tables » Layer Type Detection** . The *Layer Types Detection Template* dialog opens.



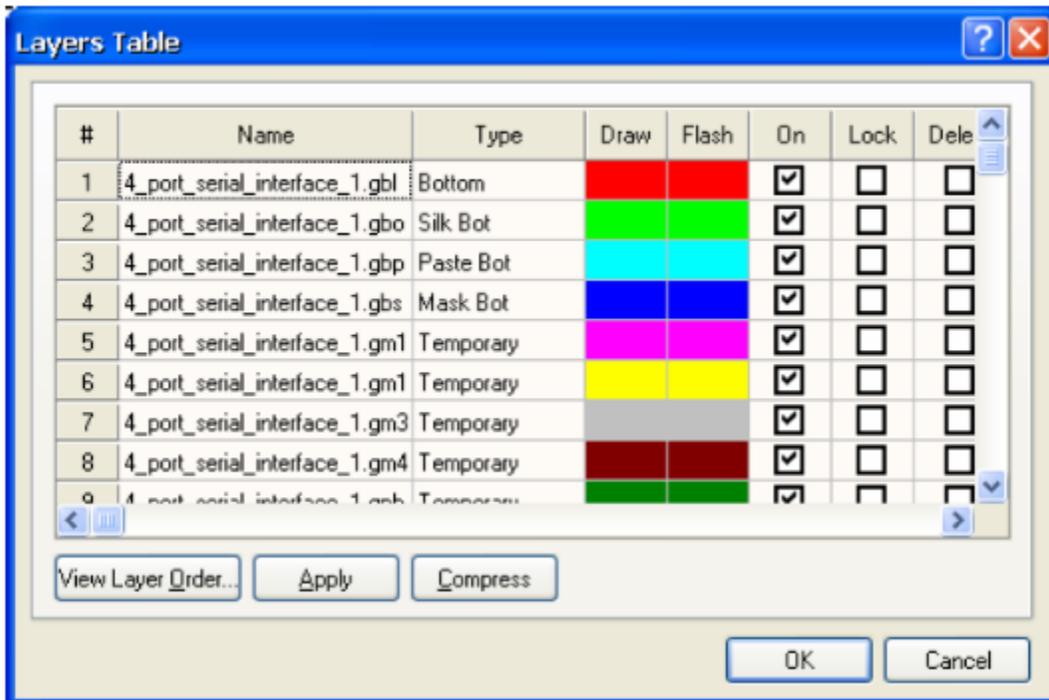
The important layers for netlist extraction, which is required before running the DRC to verify the data, are the signal and plane layers. Signal layers may be assigned to the following layer types: top, bottom or internal. Silkscreen layers will be taken into account during DRC as well.

2.If you need to add another layer type string, add a string (separated by a comma from the previous entry as shown above) to associate the layer with layer type. Note that if you have made changes to this template at this stage, you will have to re-import your files to see the new associations.

3. Click **OK** and the associations are saved with the Altium Designer environment.

Now, when we look at the Layers Table, all layers should have been assigned a layer type. To review or edit the Layers Table:

4. Select **Tables » Layers** . The *Layers Table* dialog displays.

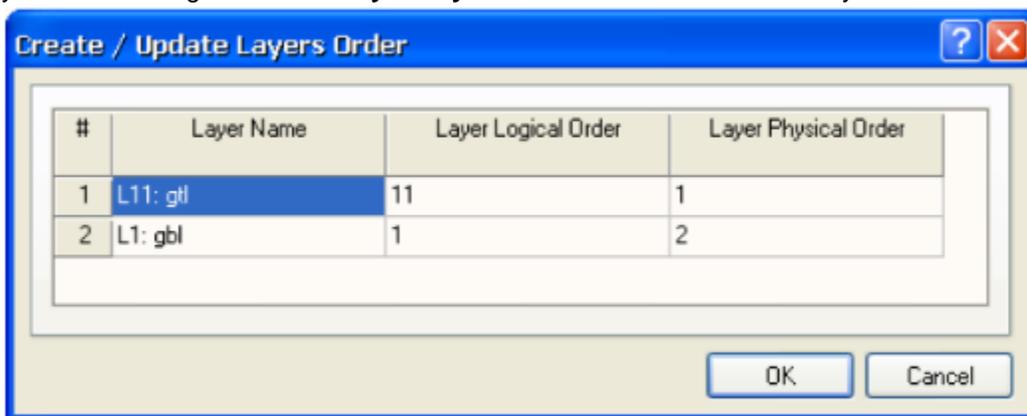


- Review the listing of layer names set up through the automatic type assignments. You will see that the layer names have been assigned to the layer types as defined in the Layer Types Detection template. Mechanical layers should be set to **Temporary**.
- Click on **OK** to close the dialog. Now we can check the layer order.

## Verify Layers Order

Once all layers are correctly assigned, you should review the Layers Order Table to ensure that the PCB layer stack is correct.

- Select **Tables » Layers Order**. The *Create/Update Layers Order* dialog displays. This dialog provides a map between the layers as they were imported into the CAM Editor (the layer logical order), and their physical build-up for manufacturing (layer physical order).
- Review the listing of layer names with automatic mapping assignments. Change the Layer Physical Order, if necessary, by clicking on the drop-down list of a layer available in this column and selecting a new value. Note that you cannot assign the same **Layer Physical Order** to more than one layer. Click **OK**.



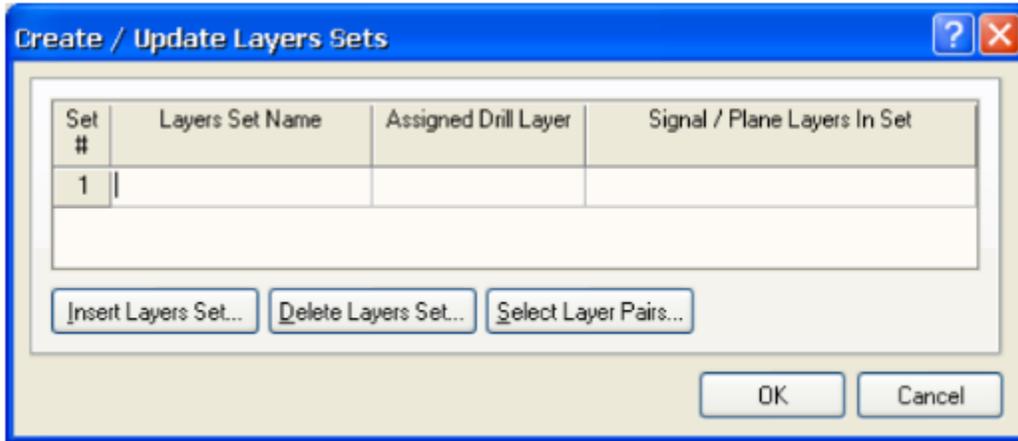
- If you close and reopen this dialog, you will notice that the stackup has been rearranged to reflect any changes to

the Layer Physical Order.

## Verify Layers Sets

Next, we could check the layer sets. This is only necessary if your board contains blind and/or buried vias, when you must designate each drill set individually, associate the corresponding NC Drill file, and select all layers through which that drill set will pass. We do not have any blind or buried vias in our example design, so you could skip this section. If you need to set up layer sets for a different design, follow these steps.

1. Select **Tables » Layers Sets** . The *Create/Update Layers Sets* dialog opens.



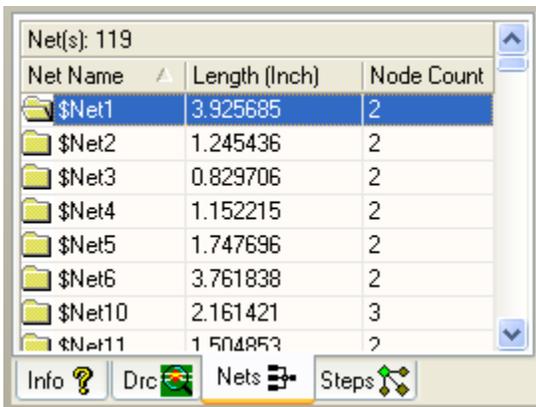
This table contains any layer pairs for associating blind or buried vias with assigned drill layers. You can insert or delete layer sets and select layer pairs from this dialog.

2. To create a layer set, type a name in the **Layers Set Name** column, e.g. Blind Top, or click **Insert Layers Set** to add a new set. Enter the data to create the Layer Sets required for the blind and buried vias in the design.

3. Select an assigned drill layer from the drop-down list that displays when you click in the Assigned Drill Layer column.

4. Select the signal/plane layers that will be included in the set from the *Select Layer Pairs* dialog that displays when you click in the **Signal/Plane Layers in Set** column. Use the **CTRL** or **SHIFT** keys to select multiple layers and click **OK** . Click **OK** to close the *Create/Update Layers Sets* dialog.

## Extract and Rename the Netlist



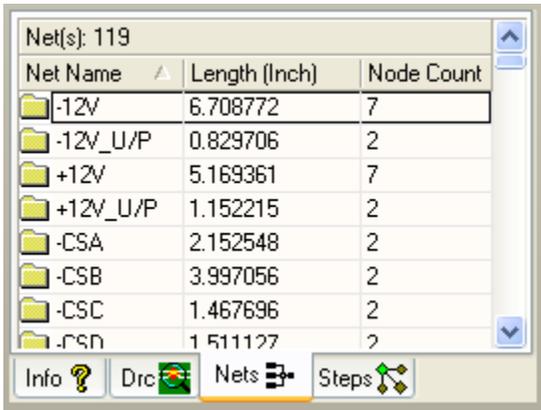
Now that we have checked the layer setups, we can create a netlist. A netlist must be extracted before you run a Design Rule Check to verify the design.

1. Select **Tools » Netlist » Extract** . The netlist is extracted. When the netlist is extracted, nets are traced along

connected copper from one layer to another according to the layer stack-up and layer sets provided.

2. Click on the **Nets** tab in the **CAM** panel to view the net names. At this stage, generic net names have been assigned, e.g. \$Net1.

## Renaming Nets



The screenshot shows a window titled "Net(s): 119" with a table of net names, lengths, and node counts. The table has three columns: "Net Name", "Length (Inch)", and "Node Count". The net names are: -12V, -12V\_U/P, +12V, +12V\_U/P, -CSA, -CSB, -CSC, and -CSN. The lengths and node counts are: 6.708772 (7), 0.829706 (2), 5.169361 (7), 1.152215 (2), 2.152548 (2), 3.997056 (2), 1.467696 (2), and 1.511127 (?). Below the table are buttons for "Info", "Drc", "Nets", and "Steps".

Net Name	Length (Inch)	Node Count
-12V	6.708772	7
-12V_U/P	0.829706	2
+12V	5.169361	7
+12V_U/P	1.152215	2
-CSA	2.152548	2
-CSB	3.997056	2
-CSC	1.467696	2
-CSN	1.511127	?

We will be able to rename the nets back to their original names in the PCB design because we included the IPC Netlist, which stores the original net names, in the Quick Load import process.

If an IPC-356-D netlist file for your Gerber and NC Drill data had not been included in the Quick Load folder, you could have imported it into the CAM Editor using the **File » Import » Netlist** command.

To rename the nets:

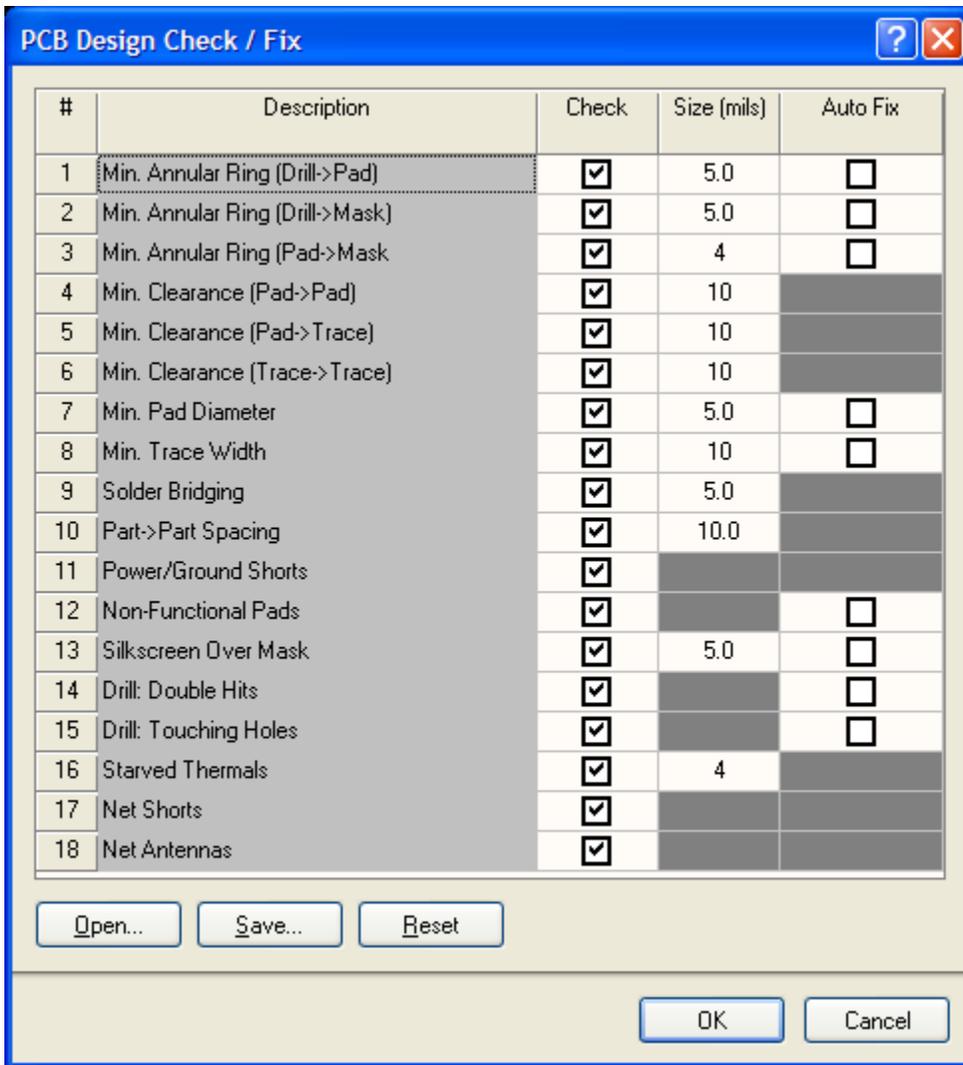
1. Select **Tools » Netlist » Rename Nets**. The net names are renamed from the CAM Editor generated nets (e.g. \$Net1) to their original names as they appeared in the PCB design, such as GND and VCC. The net names are updated in the **Nets** tab in the **CAM** panel.
2. Save the document.

## Run Design Rules Check

Now we can run a Design Rule Check (DRC) to verify there are no violations in your CAM file that will affect fabrication. You are presented with 18 rules. The values for these rules will be retained from your previous CAM Editor sessions, unless you loaded your CAM data from a Protel output that included a *.RUL* file. In any case, the values of these rules may be modified before running the DRC.

## Setting Up the DRC

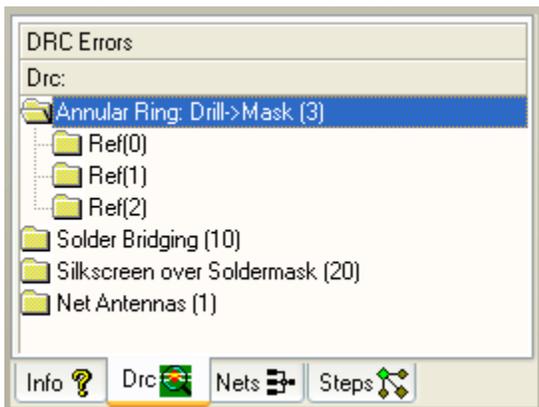
1. Select **Analysis » PCB Design Check/Fix**. The *PCB Design Check/Fix* dialog opens.



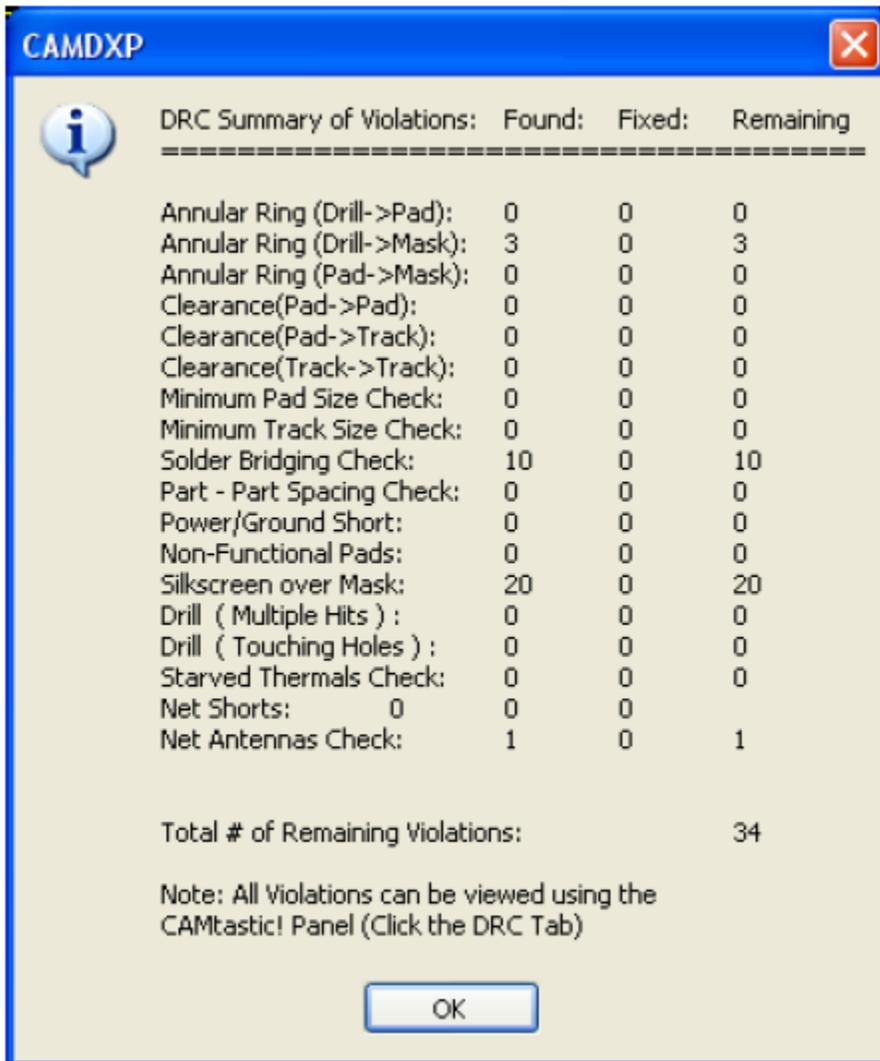
2. From this dialog, you can change relevant size values, if required, or enable the **Auto Fix** option, if available. With **Auto Fix**, the CAM Editor attempts to fix any violations found. We will first run the DRC without **Auto Fix** enabled to review the number of violations and then with it enabled.

Type in the sizes as displayed in the *PCB Design Check/Fix* dialog above. Enable all the **Check** column options. You can click on the **Check** header to toggle all options on or off.

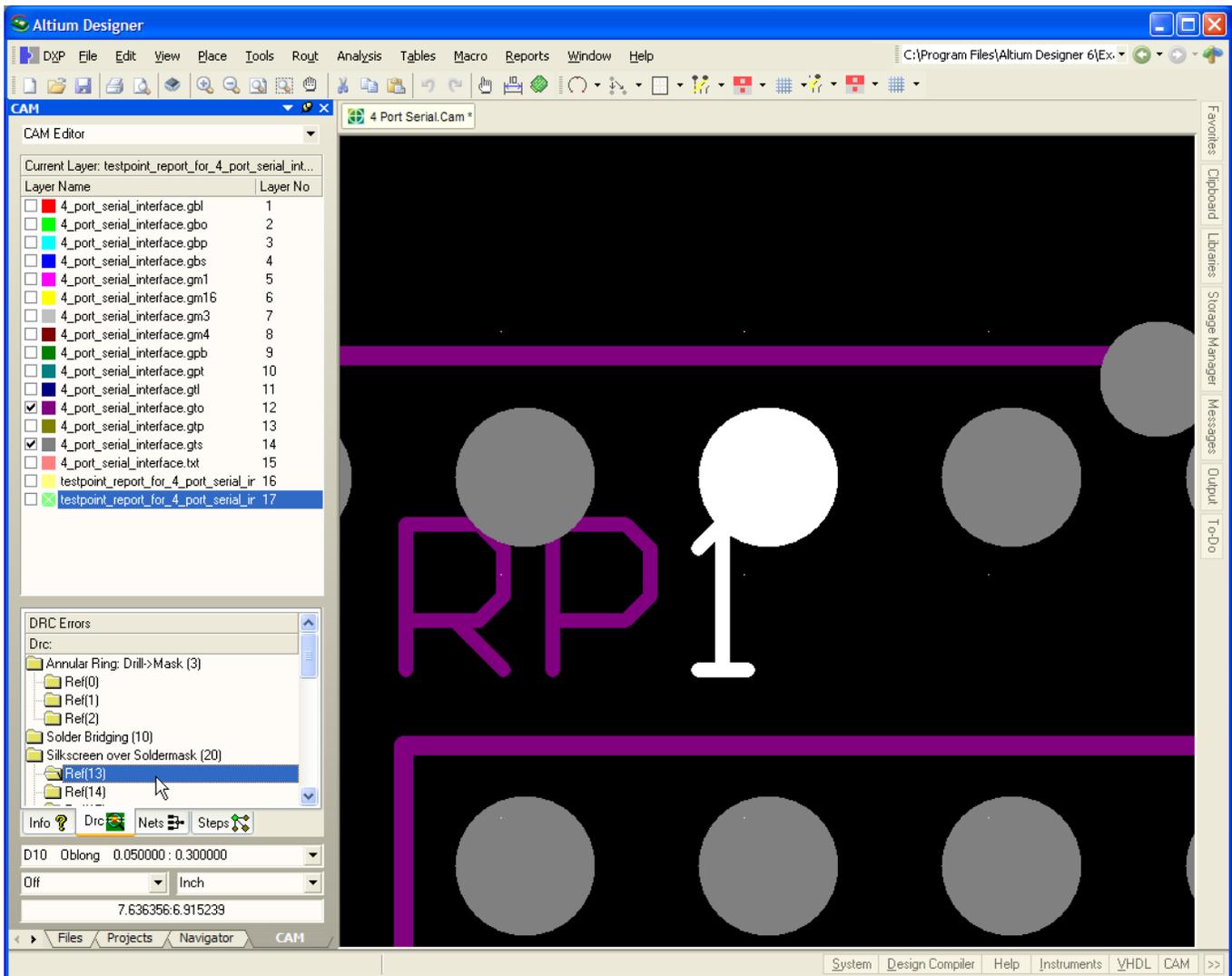
3. Once you have set up the DRC, you can save the DRC settings to a *.DRC* file by clicking on **Save**. Use the **Open** button to reload saved *.DRC* files.



4. Click **OK** to run the DRC. The DRC runs and any violations display in the *CAMDXP* dialog.



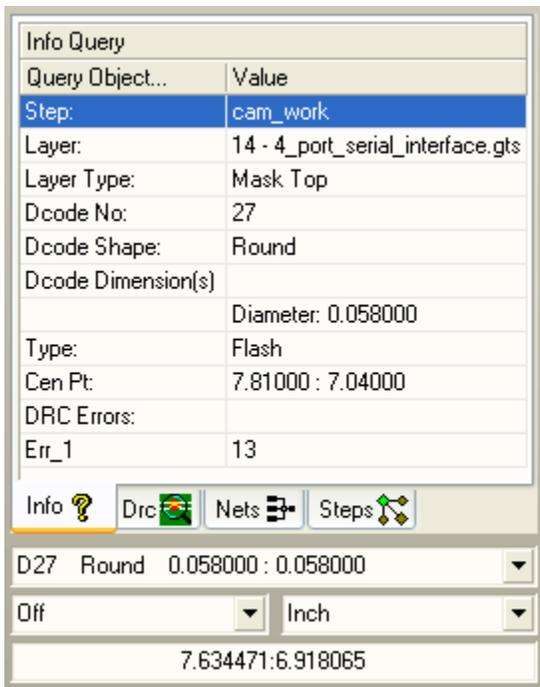
5. Click **OK** to close the dialog and click on the **Drc** tab in the **CAM** panel to view more details about each of the violations.
6. Double-click on a violation error folder in the **Drc** tab of the **CAM** panel, e.g. Silkscreen over Solder mask, to view the individual error subfolders. Click on a subfolder, e.g. Ref (13), to zoom in on and highlight the offending object/s in the design window.



## Querying a Violation for Further Information

You can find out more information about the possible reason for errors by querying the object/s involved in the violation.

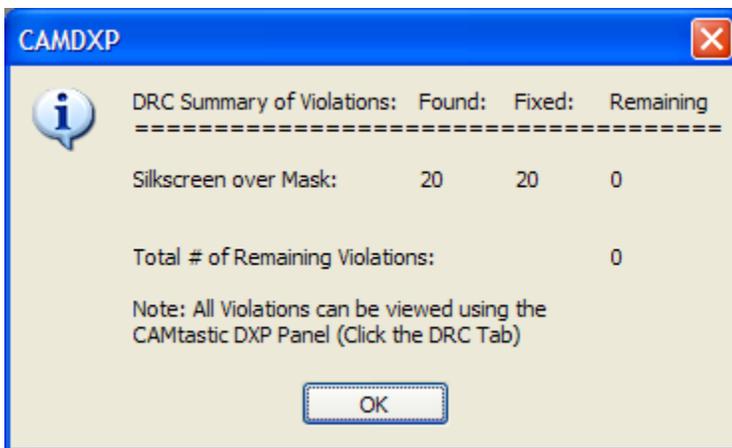
1. If the **CAM** panel is active, press **SHIFT + F5** to make the design window active, or click in the workspace. You can now use the zoom and pan commands.
2. Press **Q** for Query (or select **Analysis » Query » Object**) and the cursor changes to a pointing hand. Click on the object you wish to find more information about. The information about the selected object is displayed in the **Info** tab of the **CAM** panel. At the bottom of the Info Query section, all the DRC errors are listed that relate to the queried object. Click on these errors to zoom into those related violations.



3. You may also wish to measure distances between objects if there are clearance issues. Select a measuring option, such as **Point to Point** or **Object to Object** from the **Analysis » Measure** submenu and click on the points or objects you want to measure. The measurements are displayed in the **Info** tab of the **CAM** panel.

## Using Auto Fix

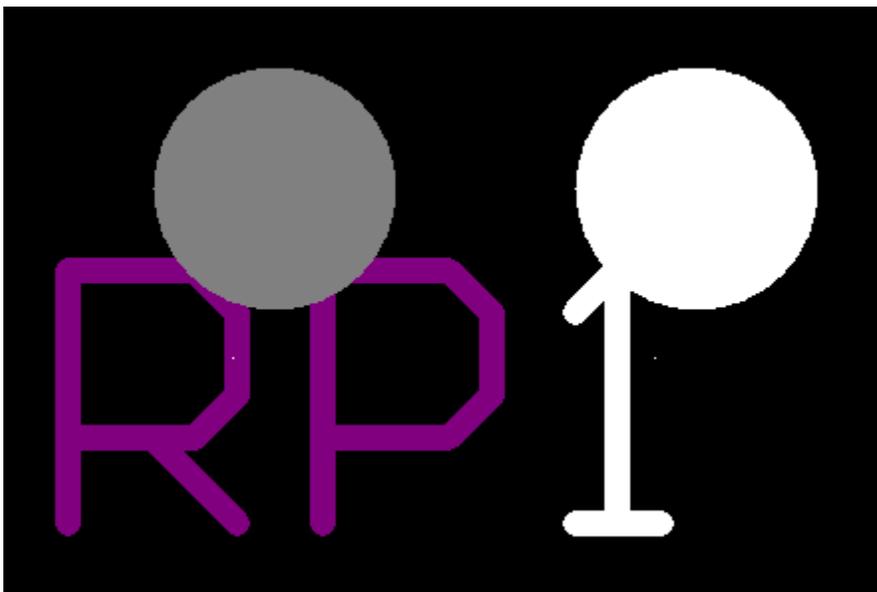
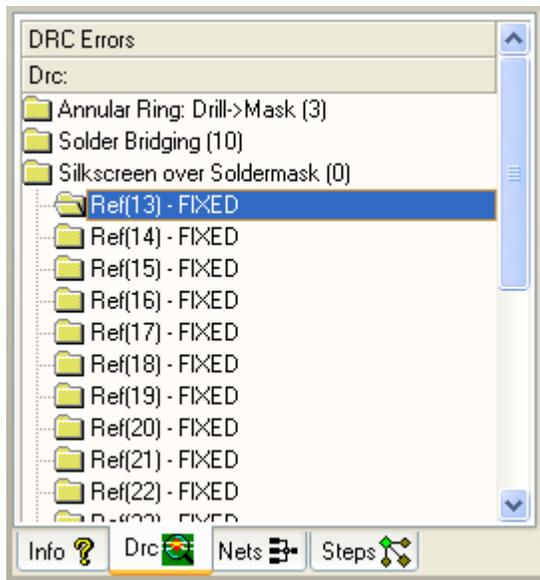
1. In the *PCB Design Check/Fix* dialog ( **Analysis » PCB Design Check/Fix** ), enable all items in the **Check** column . Enable the **Auto Fix** option for the Silkscreen over Solder Mask design rule only. Click **OK** to re-run the DRC. The *CAMDXP* dialog displays the results.



2. You will notice that number of violations has been reduced as the **Auto Fix** option has resolved the Silkscreen over Solder Mask errors. **Auto Fix** removes enough of the overlaid object to clear the violations.

3. Check what has been achieved by using the **Auto Fix** option. Double-click the Silkscreen over Solder mask violation error folder in the **Drc** tab of the **CAM** panel, then click on the *Ref (13)* subfolder to display and highlight the auto fixed objects in the design window.

4. Remember you can always use **Edit » Undo** (shortcut: **CTRL + Z**) to reverse any auto fixes.



## Using Auto Fix in the CAM Panel

You can also use the **Auto Fix** option (where applicable) from the right-click menu when in the **DRC** tab of the **CAM** panel. This allows you to fix individual errors as well as entire DRC types.

To auto fix all the silkscreen over solder mask errors, for example, right-click the *Silkscreen over Solder Mask* violations folder in **Drc** tab of the **CAM** panel and select **Fix All Silkscreen over Solder Mask errors** . All violations in that folder are fixed.

To auto fix individual errors, where available, right-click on an individual error *Ref* folder and select **Fix DRC Error** . The error is fixed.

## Checking Remaining Violations

1. Check the remaining violations and resolve any other errors as necessary. The table below explains the reasons for the remaining violations.

DRC violations	Notes
Annular Ring (Drill>Mask)	<p>The three violations are for annular rings (drill to mask) that have a negative value, which is not interpreted by the DRC. Investigation using the <b>Analysis » Query » Object</b> command (shortcut: <b>Q</b>) will show that the drill holes are larger than the pads and have a diameter of 140mil and the masks are 150mil in diameter. The drill to mask expansion of 5mil (half of the difference between the drill hole and mask diameters) is still better than the fab house minimum of 4mil (pad to mask), so these errors can be ignored.</p>
Solder Bridging	<p>Solder bridging checks the Top and Bottom layers against the Mask Top and Mask Bottom layers for the distance from the edge of the mask opening to any objects under the mask but on a different net from the pad exposed by the mask opening. DRC flags a violation if the nets are different and the objects are not correctly covered by the mask.</p> <p>In this example, the solder bridging occurs where the routing to the end connector comes in contact with the mask. Since there are many different nets under the mask, errors are generated. Visual inspection shows that this is okay, so the violations could be ignored.</p>
Net Antennas	<p>A rogue flash has been detected. This DRC looks for track ends not terminating on a track end, pad or via. This trace can be deleted by selecting <b>Edit » Clear</b> and then selecting the flash, right-click to clear and press <b>ESC</b> to end the command. Notify the PCB designer of this alteration.</p>

2. The data in the design has now been verified and the files are ready for the next manufacturing stage.