

PB01 Resources - Video Output

The PB01 supports the output of analog video signals in three formats – VGA, Composite Video and S-Video:

- Analog RGB (VGA) video output is made through a DB15F connector, designated J1.



Figure 1. VGA output connector.

- Composite Video output is made through an RCA phono jack, designated J2.



Figure 2. Composite Video output jack.

- S-Video output is made through a 4-way mini-DIN (Female) connector, designated J3, with Luma and Chroma on pins 3 and 4 respectively.

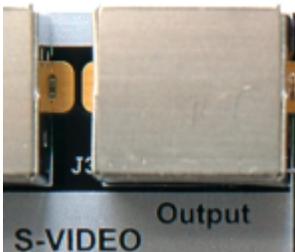


Figure 3. S-Video output connector.

VGA Output

The analog R, G and B signals – required for output to a VGA-compatible monitor – are obtained by passing the 24-bit digital RGB video signal (RGB, 8-bits parallel) through a THS8134 Video DAC device (from Texas Instruments).

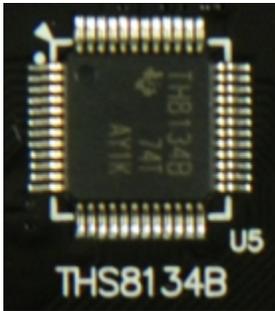


Figure 4. THS8134 Video DAC device.

Powered by 5V (analog) and 3.3V (digital) supplies, this device contains three 8-bit, 80MSPS video DACs. These are used to convert the `VGA_RED[7..0]`, `VGA_GREEN[7..0]` and `VGA_BLUE[7..0]` digital input signals generated by a VGA Controller in the daughter board FPGA design.

The device is set to operate as three 8-bit (RGB) ports by tying the `M1` and `M2` pins Low. Additional sync and blanking controls have been disabled, with the respective inputs tied High or Low as required to render these controls inactive.

Clocking for the device is courtesy of the `VGA_CLK` signal from the FPGA design. This is typically sourced from the external system clock signal to the design (`CLK_I`), which is also used as the pixel clock for the in-design VGA Controller. Data for all three input ports (R, G, B) is clocked in at each rising edge of `VGA_CLK` and all three DACs operate at this clock speed.

Each DAC uses an internally generated reference voltage of 1.35V (nominal).

The analog R, G and B outputs are subsequently passed through a voltage-feedback amplifier – a three channel MAX4382 device, from Maxim. The device is powered from the PB01's 5V supply and all channels are configured for x2 gain.

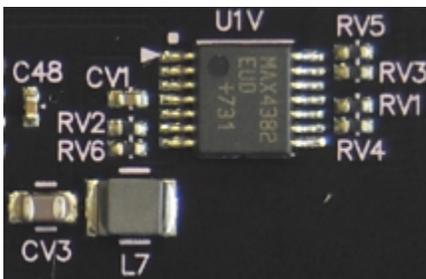


Figure 5. Voltage Feedback Amplifier, MAX4382.

The outputs of the amplifier, along with buffered `VGA_VSYNC` and `VGA_HSYNC` signals from the FPGA design's VGA Controller, are wired to the DB15 connector, for output to a connected VGA monitor. For each color, the 8-bit digital signal can be converted into 256 distinct analog levels. These levels specify the intensity of each of the three primary colors to use when displaying the pixel on a connected VGA monitor's screen. By driving each output into a 75 load prior to the connector standard video output levels are achieved, ranging from 0V (total darkness) to 0.7V (maximum brightness). With each analog input being one of 256 possible levels, the monitor can display each pixel on the screen with one of 16777216 color permutations.

Composite Video and S-Video Output

Composite Video and S-Video output signals are delivered through use of an AD725 RGB to NTSC/PAL Encoder device (from Analog Devices). Powered by the PB01's 5V supply, the encoder takes R, G and B analog signals and converts them into their corresponding luminance (Luma, Y) and chrominance (Chroma, U and V) signals, in accordance with NTSC or PAL standards. The device is permanently enabled by having tied its \overline{CE} pin High (to the 5V supply).

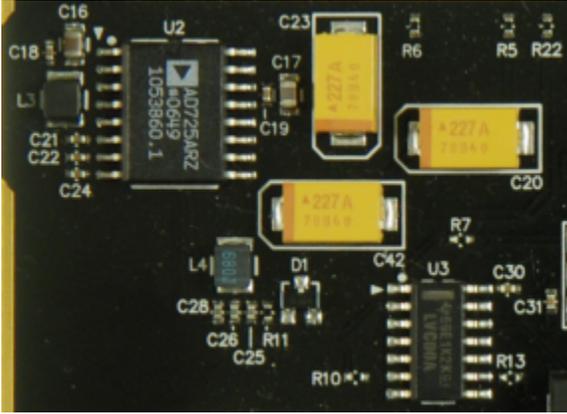


Figure 6. AD725 device (U2) and related circuitry.

The R, G and B signals routed to the AD725 device are the pure analog outputs of the THS8134 video DAC device discussed in the previous section, tapped off prior to the MAX4382 voltage-feedback amplifier.

The encoder also takes as input the `VGA_HSYNC` and `VGA_VSYNC` signals, from the FPGA design's VGA Controller. Note that the non-buffered instances of these signals are used by the AD725 device.

An additional signal from the FPGA design – `VIDOUT_NTSC_PAL` – is used to control whether the conversion involves NTSC or PAL encoding. Simply tie this signal High or Low in your design to choose between these formats respectively.

Internal timing logic is driven by an external reference frequency, which is four times the frequency of the color sub-carrier. This external frequency is connected to the device's $4F_{SC}$ pin and is dependant on the encoding standard selected:

- **NTSC** – a 14.31818MHz frequency signal is used. This signal is sourced from a dedicated crystal oscillator, which is powered by the PB01's 3.3V supply. The output of the oscillator is also buffered and sent, as the `MHZ_14_3` signal, to the `XTAL1/OSC` input of the TVP5150AM1 video decoder device (see [PB01 Resources - Video Input Capture](#)). This buffered version of the signal is also made available to the daughter board FPGA, as the `VIDOUT_MHZ_14_3` signal.
- **PAL** – a 17.734475MHz frequency signal is used. This signal is sourced from a dedicated crystal oscillator, which is powered by the PB01's 5V supply.

Test points are available for verification of both oscillator output frequencies, as well as GND.

A single NAND gate device (SN74LVC00AD, quad 2-input) provides the necessary control logic for selection between these two frequencies, based on the level of the `VIDOUT_NTSC_PAL` signal. The reference frequency is also made available to the daughter board FPGA, as the `VIDOUT_FSC4` signal.

The Chroma and Luma outputs are delivered to the S-Video connector (`J3`). The Composite output is delivered to the Composite Video output connector (`J2`). This signal is essentially the sum of the individual Chroma and Luma output signals. All outputs are driven into 75 back termination resistors, prior to the connectors.

A luminance trap filter (Y-Trap) is used to remove cross-color interference generated by sub-carrier frequency components present in the luminance signal. External circuitry connected to the device's `YTRAP` pin follows the chosen encoding (NTSC or PAL) and provides an RLC circuit tuned to nullify the luminance frequency response at the applicable chrominance sub-carrier frequency (3.579545MHz for NTSC and 4.433618MHz for PAL).

Location on Board

The DB15 connector – labeled 'VGA 24-Bit RGB' and designated `J1` – is located on the component side of the board, towards the top-right corner.

The Composite Video output jack – labeled 'Output' and designated `J2` – is located on the component side of the board, to the right of the Composite Video input jacks.

The S-Video output connector – labeled 'Output' and designated `J3` – is located on the component side of the board, to the right of the S-Video input connector.

The THS8134 device (designated `U5`) is located on the solder side of the board, below the DB15 connector.

The MAX4382 device (designated `U1V`) is located on the component side of the board, below the DB15 connector.

The AD725 device (designated `U2`), the quad NAND gate device (designated `U3`) and related circuitry are all located on the component side of the board, below the S-Video connectors.

The 14.31818MHz and 17.734475MHz crystal oscillators (designated `X1` and `X2`) are located on the component side of the board, to the right of the board's test points.

The test points for the 17.734475MHz and 14.31818MHz crystal oscillator outputs (designated `TP1` and `TP2`) are located to the left of the oscillator devices themselves.

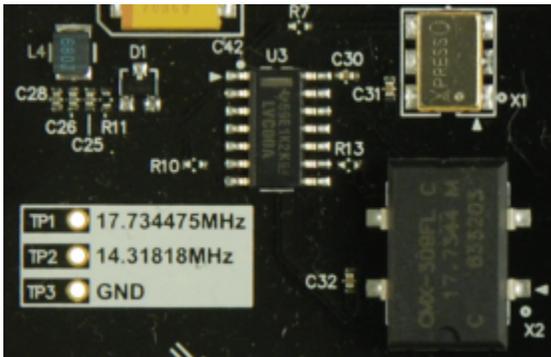


Figure 7. Crystal oscillators (`X1` and `X2`) and associated test points.

Schematic Reference

The video output circuitry can be found on the following sheets of the peripheral board schematics:

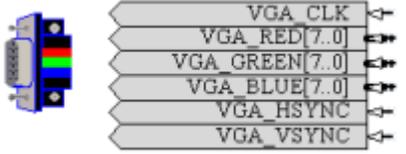
- `PB01_VGA_OUT.SchDoc` (entitled *VGA Output*)
- `VIDEO_DAC_THS8134B.SchDoc` (entitled *Video DAC*)
- `VIDEO_OUT_AD725.SchDoc` (entitled *Composite Video Encoder*)

- VIDEO_OUT_SVGA.SchDoc (entitled *SVGA Video Output*)
- VIDEO_OSCILLATOR.SchDoc (entitled *Video Oscillator*).

Design Interface Component

Table 1 summarizes the available design interface components that can be placed from the FPGA PB01 Port-Plugin.IntLib for access to, and communications with, the video output devices (THS8134 and AD725).

Table 1. Video output port-plugin components.

Component Symbol	Component Name	Description
	VIDEO_OUTPUT	Place this component to interface to the THS8134 and AD725 devices and subsequent VGA, Composite Video and S-Video output ports.
	VGACNTR	Place this component to interface to the THS8134 device and subsequent VGA port only.

Further Device Information

For more information on the THS8134 device, refer to the datasheet (ths8134.pdf) available at www.ti.com.

For more information on the AD725 device, refer to the datasheet (AD725.pdf) available at www.analog.com.

For more information on the MAX4382 device, refer to the datasheet (MAX4380-MAX4384.pdf) available at www.maxim-ic.com.