Altium Designer provides a generic set of FPGA macro components – symbolic representations of blocks of functionality that a user desires to add to an FPGA design. These components are presented to the user as FPGA-ready schematic symbols (or graphical representations in an OpenBus System) that can be instantiated into a design. FPGA-ready schematic components are like traditional PCB-ready components, except instead of the symbol being linked to a PCB footprint, each is linked to a pre-synthesized EDIF model.

The pre-synthesized components are supplied as object code entities without having to expose underlying RTL- or netlist-level source code. The system includes multiple libraries providing a comprehensive set of pre-synthesized components, ranging from simple gate-level functional blocks, up through high-level hardware functions, such as multipliers and pulse-width modulators, to high-level functions, such as processors and communications peripherals.

These components can be instantiated into designs by the system user and then the whole design can be targeted to a suitable physical device. Altium Designer automatically manages the resources required to instantiate the design in the chosen FPGA device, by ensuring that the EDIF models specific to that device are correctly chosen and linked to the generic symbols placed when capturing the design.

The result is a design environment that offers true device vendor independence, with the ability to quickly retarget your FPGA design to a different device with relative ease.

**Model Linkage Mechanics**

**Tutorial - Creating a Core Component**

**Generic Logic**

[FPGA Generic Library Guide](#)

**Peripherals**

[Wishbone Components](#)

[Non-Wishbone Components](#)

**OpenBus System Components**

[OpenBus Interconnect Component](#)

[OpenBus Arbiter Component](#)

**Working with Hardware Description Languages**

[VHDL Language Reference](#)

[VHDL Synthesis Reference](#)

**Core Resource Usage**

[FPGA Arithmetic Function Resource Usage](#)
FPGA Buffer Resource Usage
FPGA Bus Joiner Resource Usage
FPGA Clock Divider Resource Usage
FPGA Clock Manager Resource Usage
FPGA Comparator Resource Usage
FPGA Counter Resource Usage
FPGA Decoder Resource Usage
FPGA Encoder Resource Usage
FPGA Flip Flop Resource Usage
  FPGA Instrument Resource Usage
  FPGA Latch Resource Usage
  FPGA Logic Primitive Resource Usage
  FPGA Multiplexer Resource Usage
  FPGA Numeric Connector Resource Usage
  FPGA Peripheral Resource Usage
  FPGA Processor Resource Usage
  FPGA Shift Register Resource Usage
  FPGA Shifter Resource Usage
  FPGA Wired Function Resource Usage

See Also

**Soft Design**

**Processor-based FPGA Design**

**Altium Hardware**