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Altium Designer 10 Base Platform (Platform Build 10.391.22084) – February 24, 2011

PCB

50	The memory utilization of Altium Designer has been improved by separating the generation of visual meshes of STEP models into a separate system process.
87	Mechanical Layers beyond 16 are now displayed in the Update From Libraries comparison list
185	Examples folder has been moved out of the Program Files folder to prevent security issues in Vista and Windows 7
192	Fixed typo in Messages panel for Testpoint Rule message
261	The behaviour of "Jump to Component" dialog has been fixed. Now the entries in the components list are no longer truncated to 18 chars. The dialog title was also changed to "Placed Components".
272	Saving a PCB document to ASCII will no longer strip out the embedded board objects
278	Only relevant files are opened in CAMtastic® after creating a Testpoint Report from PCB
287	Altium Designer STEP model functions are no longer affected by a small number of third party STEP viewer applications.
364	Minimum Mask Sliver DRC errors will now be correctly generated for pads rotated 90 or 270 degrees.
372	Rule Wizard dialog has been updated. Now the text fields on 1st & last page are no longer editable. The caption at the top of each page is no longer cropped & the dialog is now no longer sizable so the picture at the top will not disappear anymore.
396	Selecting and dragging of tabs in a SimView Wave document now works correctly when there are many tabs and the first is not visible.
428	Problem parsing Spice resistor temperature coefficients was fixed.
435	Starved Thermals DRC error check has been improved. No fake DRC errors will be generated anymore for available copper area less than 50% from the ideal copper area.
454	The "Set Snap Grid" dialog can now toggle units
474	The Export to PCB command has been improved. Now any existing split planes within enclosed polylines will be correctly exported to PCB
504	Gerber files for Mechanical Layers 17 to 32 will now import into PCB through the File>Import menu
524	The use of Panelization option when generating Gerber output has been corrected. Now the selected layers will be correctly panelized & the generated Gerber files will be loaded in CAMtastic® if auto-load option is turned on.
541	The ODB++ Output generation has been improved. Now the generated directory structure will be zipped into one file that can be added to version control more easily & the .svn folder will not be removed anymore.
553	Object Class Explorer has been improved. The Add Selection command no longer selects an extra item in the list. Also the speed with which the lists are populated has been improved as well.
555	PCB Preferences>Board Insight Display page - Font Name and Style now update correctly in DirectX mode
567	The Edit Rule Priorities dialog for PCB Rules can now be resized.
665	Pressing SpaceBar will no longer reset the HUD delta origin while in interactive processes
718	When repositioning components an warning will be shown if any of the components is locked.
727	The reference point for placing and dragging 3D bodies will now be their origin
728	Adding snap points during initial placement of 3D bodies will now work
741	In certain situations, dimensions were lost when saving a PCB to ASCII. This no longer occurs.
770	In DirectX mode, hitting END will now flush video memory
815	The modified status of "DRC Violations Display" page will now be reset after applying the changes
825	Rooms will now snap to each other as they did prior to S09.

826	The internal split planes imported from 99SE will no longer miss their nets.
828	When alignment tools are used to align component text, only the text is aligned now instead of the whole component.
887	The support for PCB Mechanical Layers 17 to 32 has been improved in the Scripting System.
902	ODB++ output EDA/data sub net (SNT) records will now contain lines for linking the drill features with the sub net records. These lines have the format "FID H Layer# Feature#".
905	The reference scripts have been updated to include support Mechanical Layers 17 - 32 where appropriate.
906	The MaxMin Width Constraint has been improved. Now the constraint will also check nets that have only pads & vias on the current layer being checked.
914	Access Violations no longer occur when trying to explode STEP models.
955	Routing in 45/90deg Arc mode no longer starts the next un-committed arc from the start point of the previous arc instead of the end point.
1012	Adding teardrops to pads and vias no longer requires a longer track length than in version AD6.9.
1121	Teardrop Options Dialog now reads the correctly with regards to Pads and Vias being teardropped.
1374	When editing the edges of polygons and regions floating panels will now go transparent as the cursor moves nearby, as is the convention when interacting with the PCB.
1385	The interactive route tool was not properly auto-terminating when clicking over a same net object if the electrical grid was off.
1386	The converted .Designator special string is no longer locked until the corresponding component or designator are moved.
1387	Fixed the interactive route tool to not leave overlapping tracks when starting a route from a track but not at the track's endpoint. Additionally, the tracks may not have been combined into a single track if the tracks are parallel.
1388	The speed of split planes rebuild & loading has been improved between 2 & 4 times compared with S09. The speed of split planes editing has been improved between 10 & 20 times compared with S09.
1389	Improved the SMD pad entry tracks in the interactive route tool.
1390	Imported Protel Version 2.7 and 2.8 designs did not use the correct pad stack layer sizes and shape when pads were specifically bottom layer SMT pads. This issue has been resolved.
1391	After modifying a plane layer by double-clicking on its layer tab, the plane did not always properly update. This modification now operates more consistently with modifications completed using the Layer Stack Manager.
1392	The Interactive Routing Options form had an incorrect text of "Push Modes" next to the "Follow Mouse Trail" label. Follow Mouse Trail works with Walkaround Conflicting Objects as well.
1393	Now "Copy Room Formats" will copy any copper pour polygons solid or hatched when "Enclosed & Touching Objects" options is set. Also there will no longer be a crash when hatched polygons are copied this way.
1394	When modifying properties of either a Fabrication or Assembly Testpoint Style rule, the Allowed Side Top/Bottom checkbox options can now be successfully used to constrain the testpoint board side.
1395	The interactive Multiroute and Diff Pair tools would sometimes not use the existing track width when the option "Pickup track width from existing Routes" was checked.
1396	Remove the 'Background' layer from the layers dialog that erroneously appeared in the Winter 09 release.
1397	Short/Medium/Long Display name setting for the layer tabs is now remembered between Altium Designer sessions.
1398	IPC-D-356A testpoint reports were not including assigned testpoints for proper generation of testpoint (099) records in the output file. This has been corrected.
1399	After setting a Solder Mask Expansion rule's scope as OnBottomSolderMask, Altium Designer could produce a fault followed by an abnormal termination. This issue has been corrected.
1400	Added support for Loop Removal in Interactive Diff Pair and Multi-route tools
1401	A bug has been fixed whereby pads containing non zero hole rotations or non zero Offsets were incorrectly mirrored.
1402	A new Coordinate Positions option has been added to Testpoint Report Setup. The new option allows all testpoint report formats (including IPC-D-356A) to be exported relative to the absolute board origin or the current board origin.
1403	Routed net lengths and manhattan lengths greater than ~214750mil (5454 mm) are no longer displayed as negative lengths.

1404	Now the Net Antenna violations will update when a component is moved if needed.
1405	Improved glossing of diff pair tracks so that tracks in the diff pair are not moved such that a larger gap than specified by the rule is not created.
1406	Apostrophe's are now included in the Query Helper results for objects with a name specifier.
1408	Added "Allow Via Pushing" option to interactive route tool.
1409	All testpoint report types now support embedded board arrays. Multiple IPC-D-356A netlist files are produced when exported from a PCB document that contains multiple embedded board arrays.
1410	A problem in the layer stack manager has been fixed whereby it was incorrectly adding a MidLayer31 to the layer stack.
1411	SMD To Plane Rule has been improved. Now the distance between the SMD pad & the closest via is correctly calculated. Now the rule takes into account only the vias that connect to a split plane that has the same net as the SMD pad.
1412	Changing Designator/Comment properties no longer very slow if the PCB Document contains hatched polygons.
1413	Fixed a case in the Interactive Route Tool when the route mode is HugNPush and attempting to hug two traces that form a convex corner would sometimes cause a small, incorrect push of one of the traces.
1414	The display of BarCode text for special strings has been rectified. Now the text will appear underneath the barcode always.
1415	Testpoint DRC should now give correct results for vias with varying sizes through the via stack
1416	When viewed in 3D pad holes that are larger than the pad copper cut into the solder mask.
1417	Now Net Antenna Rule will no longer create bogus violations for small tracks of different widths.
1418	"Copy Room Formats" command no longer duplicates polygons.
1419	Accessing and using the Favorite Interactive Routing Via Sizes dialog through system preferences with no PCB design currently open could cause a system fault in Altium Designer. This issue has been corrected.
1420	Crash when enabling layers caused by coordinate object that lost its text member no longer occurs.
1421	All via stack layer sizes are now preserved when saving even if the layers don't exist on the PCB
1422	After choosing via sizes during interactive routing, the tool would sometimes place a via that respects the selected hole size, but not the other via size features. This issue has been resolved.
1423	When an ASCII PcbDoc that contains split planes was loaded into the PCB Editor, the split planes were not retaining their individual net assignments. This issue has been resolved.
1424	Fixed cases where a via could not be pushed when clearly there are not obstacles in the way.
1425	Right Reading, Autopositioning and Text Justification have been improved for imported P-CAD PCB designs
1426	Saving a PCB document in ASCII 2.8 format no longer changes the SMD Rounded Rectangular pads placed on Bottom Layer in the Original File to Rectangular pads.
1427	Improved the Interactive Routing "Follow Mouse Trail" mode so that the tracks stay in the user indicated path when going around an obstacle and do not "jump" over that obstacle.
1428	Use of Design Rule Checker dialog was marking PCB design document as out-of-date, regardless of whether any design data was modified. This has been corrected.
1429	Now any pads/vias that touch will also be considered connected so they will appear in the Gerber/ODB++ output even if the "Include unconnected MidLayer pads" option is not checked.
1430	In the interactive route tool, improve the results when routing between vias so that one of the vias is pushed rather than moving the route to the outside of the vias.
1431	Added 2 new Condition Types to Query Builder: "In Any Polygon" - targets the member objects of any polygon in board (translates to InPolygon) & "Belongs to Polygon" - targets the member objects of a named polygon (translates to InNamedPolygon('Poly Name')
1432	Clearance Rules are now ignored for objects that are members of the same Differential Pair. Instead of using Clearance Rules for such objects, the Differential Pairs Routing Rule's Min Gap value is used to constrain differential pair object clearances.
1433	Fixed the interactive router so that after using the "Swap To Opposite Route Point" (shortcut of '9') and terminating the route, the route object (via, track, or arc) added before the "swap" command is not left in a locked state.
1434	SMD NeckDown Rule has been improved. Now this rule will check only the SMD pads instead of all pads.

1435	Fixed the Multi-route tool and Diff-pair tool used with obstacle avoidance set to Stop At First Obstacle mode to not cause violations.
1437	When using InFromTo( ) in Query Helper, a selection of existing FromTo specifiers should auto popup for selection, but the popup is absent. The popup behavior for FromTo selection has been fixed.
1457	Now CAMtastic® NC Rout loader will correctly import rout paths containing counter clockwise arcs. Also the correct cutter compensation will be used even if not specified in the tool selection command.
1458	Polygon definitions that do not fully follow the Gerber standard (e.g. G36 definitions followed by G54 aperture selection command) will now be correctly loaded in CAMtastic®.
1459	The CAMtastic® Gerber loader has been improved. Now the loader will be able to load malformed polyline aperture macro definitions that have less points defined then the count specified in the macro definition.
1460	The NC drill export of embedded board arrays have been improved. Now any mirrored embedded board arrays containing blind/buried vias will be correctly exported.
1462	An AV no longer occurs if IKF is not specified in a PSpice diode model.
1485	When running the Design->Make PCB Library command component bodies that contained STEP models would be misplaced in the pcblib. This issue is now resolved.
1517	Cycling through signal layers will now work correctly. If the next layer is an Internal Plane layer then the next signal layer will be made current.
1622	The right click menu command "Wrap Rectangular Room Around Components" will now work on all selected rooms.
1636	Fixed issue when copy and pasting a mirrored embedded board array whereby it would unmirror
1638	A bug has been resolved whereby the mask shown in the "PCB Library Navigator" panel for pcblib's would incorrect display '*' despite the list of components been filtered by an active mask.
1663	The PCB Navigator, Rules & Violations & 3D Models panels "Mask" mode with selection has been fixed. Now the selection no longer persist when turned OFF & the panel mode is set to "Mask"
1679	The PCB Panel and PCB Library Panel have been improved so that they now use the user defined layer names.
1684	Correct file extension used when saving STEP files under Windows Vista and Windows 7, thus preventing overwriting original PcbDoc file
1689	The density map now works in DirectX
1692	Improved show up time for Pop-up ambiguity resolution menu on large designs
1696	Now the lengthy delays seen when moving text caused by unnecessary update of power plane connections has been corrected
1708	Floating Panels blending has been fixed for interactive routing
1709	In the PCB Library editor, use of the FSO now has the Whole Library option unchecked by default.
1720	Export to SiSoft Files option has been added to the file types available in the PCB save as dialog.
1737	Improved show up time for Layers/View Configuration dialog on large PCB designs
1742	Improved cursor hit testing performance on large designs
1790	Favorite interactive routing sizes now has fields which will update correctly by clicking the OK button without having to change fields first.
1797	Export Ansoft Neutral File (*.anf) was added as an option to the PCB file Save As dialog.
1806	Reimplemented glossing of connected tracks when via is dragged.
1807	Fixed a long startup delay in the Interactive Router. The delay could occur if shorts to large nets existed in the design, typically caused by out-of-date flooded copper pours.
1813	When the reference location for a component in a PCB library editor is changed and the library subsequently saved a redraw issue occurred whereby the component would appear to jump around. This issue has been fixed.
1814	The PCB Layer Sets will now be updated after Update from Libraries
1818	Erroneous "Isolated Copper" DRC errors that were produced on boards with internal planes have been fixed.
1824	Hitting ESC now works to cancel the Applicable Rules dialog.

1828	In the PCB Panel, the zoom level popup dialog now stays within the screen
1831	Unit suffixes have been removed from values in the PCB Panel and PCB List and now appear in the column title where appropriate.
1849	The solder mask now updates after modifying the board outline in 3D
1876	The "Import" sub-menu in PCB library will no longer be visible if empty (no commands associated with it)
1898	Fixed crash in diff pair length tuning process, when tuning code could not find solution
1917	CAMtastic® Export 2 PCB process no longer creates extra multilayer pad in origin
1932	Now component/net classes will Undo/Redo correctly after ECO
1974	Exported boards as step now are positioned in external step programs at (x=0,y=0,z=0). Solder Masks are now taken into account upon export
2013	Delays after zooming or panning large PCB designs have been removed
2035	SimView print now uses the scale values specified in the plots.
2042	Allowed for Copy/Paste and Place in 3D mode
2049	There is a new anti-aliasing option to allow higher quality 3D outjobs and views
2051	In 2D DirectX, pads with square or slot holes will now display their internal plane connection relief patterns properly
2064	Copy and Pasting a Footprint in the PCB editor will no longer create duplicated UniqueID's
2073	Pads placed on silkscreen layers will now appear in 3D
2081	Textures on locked objects now works and obeys the chosen preferences
2094	The behaviour of copy and pasting primitives that belong to unions had been changed so that the newly pasted primitives are not added to the existing union.
2107	CAMtastic® printing has been corrected. Now will print the header text on each page instead of only on the 1st one
2109	Now Pad/Via relief patterns will change to draft drawing when in Draft mode.
2158	Make user selection persistent (store No net Objects/Locked Objects flags) during an AD session & also show this dialog always only if the user choose to do so
2199	Now BGA Escape Route will follow the width rule as expected
2204	Move/Rotation of embedded board now respects input point location, instead of rotating about embedded board origin.
2215	The speed of the "Update selected components from PCB libraries" command has been improved.
2217	The speed of Polygon editing for polygons with large number of vertices has been improved, now the process is on average ~100 times faster than before.
2222	TrueType text now displays the letters that have voids in them correctly
2223	Now the rounded rectangular pads mask corner radius will be calculated using the full mask expansion instead of a percentage of it
2239	Improved memory usage by solid polygon and polyregions by factor of 2
2272	Any changes made to "Board Insight Color Overrides" properties page will now be applied & the page will no longer be marked dirty
2273	"Make PCB Library" command will copy all text properties including the TrueType Text & BarCode text ones
2275	Measure Primitives now additionally reports the "corresponding layer distance" when it is different from the "flattened layer distance"
2299	The "Measure Primitives" now works with polygons.
2366	Changing the pattern or zoom-out behaviour of DRC violation overlays no longer needs to rebuild the scene
2395	In 3D, the transparent side walls of board cutouts will now always display properly, objects within cutouts will now be visible, and flying the camera into a cutout will not glitch.
2413	The Layer tab right click menu now correctly shows whether the board is flipped.
2435	The "File in Previous Format" warning report no longer gets added to the wrong project.
2447	Hatched polygon repour no longer includes overlapping copper

2458	The Ibis converter has been updated with version 5.0.3 of the ibis golden parser
2467	Improved detection of starved thermals when multiple disconnected copper islands are present on internal plane
2475	Now the Routing Width set through Diff/Multi-route TAB key dialog will be used similar with the single trace router
2477	Routing Cross Hair no longer disappears when exiting nested processes & returning back to routing
2488	Hitting ESC now Cancels the "Object Class Explorer" dialog
2489	Changed the arc handle modification so that the start and end points remained fixed. The original mode, whereby the start and end points would move, is accessible by holding down the ctrl key.
2495	Grids will no longer become dimmed or masked
2550	The shadow will longer flicker on the first frame or after rebuilding the scene
2629	The PCB List/Object Inspector "Objects to Display" pop-up will no longer truncate the objects kind list on Windows 7 with Medium Fonts.
2652	CAMtastic® Gerber loader has been improved. Now 3rd party Gerbers containing polygon definitions will be correctly imported.
2673	Fixed possible lockup in Interactive Router during push operations and a specific track geometry.
2674	Loop Removal for the Interactive Routers now works when routing across an open circuit and removes any leftover stub.
2683	Small tracks within vias can now be dragged.
2684	Loop removal of the Interactive Router no longer incorrectly removes a via when routing to that via.
2688	Board Level Libraries for Actel SmartFusion devices are now available.
2694	An issue has been resolved whereby the footprint selected in the pcb library list would not match the visible footprint in the PcbLib editor immediately after running the IPCÂ® Compliant Footprint Wizard.
2699	The Polygon Manager will now recognize that a change to the Pour Order requires a repour of affected polygons.
2721	Fixed Interactive Router to not potentially leave a stub track behind when in lookahead mode. The stub track was left if the user left-button clicked to commit a route, then immediately right-clicked to quit the route without moving the mouse.
2724	A small pause after saving PCB documents has been improved. The pause was caused by the generation of the PCB document preview used by the design insight feature. The generation of the preview has been optimized and is now 50% faster.
2763	A crash should no longer occur while running Batch DRC if the user clicks in the "PCB Rules and Violations" panel
2771	The Make PCB Library command from PCB Editor now more precisely replicates component pad shapes and sizes when the padstack mode is set as Top-Middle-Bottom or Full Stack.
2772	PCB FSO will no longer throw an error when "Lock Strings" attribute value is changed & the filter applied
2782	Un-routed net violations will display the net name in violations panel & the violating primitives will display fully when zooming into the violation from violations panel
2784	The Temporary Mesh Data in the preferences->pcb->models is now created if it does not exist on the disk.
2785	ODB++ no longer fails to generate output from a PCB document when the pad shape information is incorrect because the pad shape size is 0, e.g. Mounting Holes where only the Holes Size is defined.
2788	Unplated pads are now correctly reported by Unrouted Net (a.k.a. Broken Net) rule when internal planes are present on the board.
2803	Make PCB Library command now auto-adds created PCB Library to PCB project, when appropriate.
2807	The "Wrap room around component" family of commands now work when the rule that a room targets is not enabled in the rules dialog.
2808	An issue was fixed when panning the PCB editor view with the SpaceNavigator device. If the mouse cursor was positioned over the horizontal scroll bar in the PCB editor the pan direction was previously incorrect.
2824	Place String command no longer fails if the mouse position doesn't change and the old/new text x1,y1,x2,y2 are the same.
2835	PCB ASCII format loader will now import Top/Mid/Bottom stack pads correctly
2866	If the folder defined for Temporary Mesh Data in preferences is not writable, a message is now displayed in the Messages Panel.
2873	Now the Default Primitives Layer will be able to be selected from all possible layers for that specific primitive

2881	PCB Editor's Teardrop tool now creates teardrops for routed arcs that connect to pads and vias.
2907	The multi-route tool no longer leaves a no-net start object in a state that can cause a crash.
2922	"Deselect / Inside Area" command will now deselect the board outline if it was selected
2926	Designator / Comment Locked flags are again working as expected in PCB Inspector & PCB List panels.
2934	The pad selection display in the component preview in "Configure Pin Swapping For Component in Project" dialog will no longer be obscured by the masked component bodies
2938	An Access Violation will no longer occur in "Pin Swapper" dialog when grouping the rows of the "Pin Swapping" grid by "Pin Group", selecting some of the rows & then click on the component preview window
2985	The short-cuts list shown by pressing F1 key while in any of the interactive processes will no longer include the menu item separators (SEPn).
2999	Query Helper and Query Builder now consistently enclose all name strings that users select from hint helper popup menus in single-quotes.
3015	Solid regions will now dynamically pick up nets as they are placed.
3021	Changing the Text Height when using "Place Text" command will now take effect immediately.
3028	The Interactive Router no longer potentially leaves a track in a locked state after a push.
3074	"Layer Stack Manager" layer stack kind drop down box is no longer editable if focused.
3075	An AV no longer occurs when exporting a PCB document to Specctra CCT in Windows Vista - Windows 7 if the user doesn't have Administrator rights.
3095	"Explode Polygon to Free Primitives" command (for Solid Polygons) no longer creates polygon regions that are not editable & could disappear when the PCB document is saved.
3100	Dragging Track End with "Preserve Angle When Dragging" option ON will no longer remove the dragged track if its length is <= than the track width.
3108	SMD to Corner Rule no longer creates bogus violations if multiple tracks intersect inside the SMD pad
3109	The PCB library Panel components filter (Mask combo-box) has been improved. Now the wild card will be automatically appended if needed & the filter will happen after each key press so there will be no need to press Enter.
3116	Gerber Output for drill symbols on Drill Drawing Layers no longer uses very big apertures that can make the user believe that there is some error or randomness in the Output.
3139	The View configurations editor Apply button will now update Color changes as expected.
3166	The crash that used to occur when running Acute Angle DRC rule for designs containing big hatched polygons has been fixed.
3197	Improve the auto-picking of the neighboring differential-pair primitive in the Advanced Differential Pair route tool.
3214	The loop removal logic of the Interactive Router no longer removes a necessary short track that is completely inside a via or pad.
3215	The loop removal of the Interactive Router no longer removes regions.
3250	The Interactive Routers no longer treats polygon pour outline objects (from an unfilled polygon pour) as obstacles. This was causing vias to be pushed potentially much larger distances than necessary.
3281	Interactive route now avoids net cleanup step when no routes have been committed.
3337	The default maximum font size for net names has been increased from 20 to 40
3343	Default setting for polygons are now applied to polygons created from primitives as they are changed from outline to Solid.
3381	PCB Editor's Make PCB Library utility now respects XY offsets of component pads when building library component footprints.
3392	An AV in "PCB Rules & Violations Panel" will no longer occur after running an ECO that will remove nets from pads that have "UnRouted Net" Constraint violations.
3490	The error that used to occur when loading Gerber files in RS 274X format containing parameterized macro apertures has been fixed.
4011	In some situations extruded 3D bodies could jump to the origin after editing their properties - this has been fixed
4077	3D bodies will now update properly when 'prefer simple' or 'prefer STEP' is selected in the view configuration

4156	A bug where the option PCB Editor -> Board Insight Display -> Minimum Object Size appeared to be capped at 10 is now fixed
4162	The speed of Clearance & Short Circuit DRC checks has been greatly improved.
4263	The addition of simple bodies to a step in a library component will now update correctly to the pcb document.
4298	An assertion failure that occurred when editing the QMatrix button has been resolved.
4378	Extruded 3D models with same Standoff and Overall heights will no longer produce critical crashes

Schematic and System-level

11	The borders of panels have been improved in Windows 7 and now draw correctly.
12	Examples have been move out of Program Files to allow them to be run on Windows 7 without admin rights.
64	What's This Help under Windows 7 now shows correct warning when is not installed
77	Publish to PDF now displays an information message rather than an error when Adobe Reader is not installed
84	List of missing Device Sheets is truncated if necessary to avoid error dialog exceeding screen size.
174	When script is stopped, evaluate dialog (Ctrl+F7) is processing Tab key correctly now and focus does not stay on the same control
182	EnableBasic scripts now display the script names correctly and can be executed.
184	The Edit Command dialog will now always stay on top of the Customizing Editor dialog when editing a process launcher.
187	The smart edit function from the Inspector has been improved. Now target text can be left empty allowing sections of text to be removed from all selected objects.
193	Code completion for Delphi script is now populating expected methods for functions returning an object.
206	Comparator engine has been optimized to significantly enhance performance of update PCB from Schematic for some Multi-Channel designs.
209	Ctrl+Delete keybinding that deletes text to the end of the word, is added to text editors
210	The Libraries Search dialog now applies the SQL quoting options of DBLIBs correctly, fixing errors when searching Oracle databases.
211	Filtering in DBLIBs that use Oracle databases now works.
212	A crash has been fixed, for Database Libraries that are Grouped in the library panel while using tables containing different column layouts (schema).
267	Memory leaks when updating PCB from Schematic document in multichannel designs have been fixed.
273	Memory leaks when comparing physical PCBs have been fixed.
286	Creating reports in To-Do panel with a single To-Do entry now works correctly.
300	Radio and checkbox controls are now rendered at the correct size when using Medium - 125% Display Settings in Windows 7.
304	Fixed port direction when port is connected directly to pin, with no wire/bus in between.
324	When Bill of Materials includes Not Fitted components, the varied values will now be used in the report.
325	OpenBus sheets can now be selected from the Sheet Symbol properties dialog
336	Now all the PCB Preferences pages will scale the controls according with the current size of the font (standard, medium, larger in Win7) & also current screen resolution
337	Various dialogs have been modified to display correctly when the Display is set to Medium 125% in Windows 7.
339	Closing document tabs using Ctrl+F4 keys is now more reliable.
343	Inspector Panel and Component Properties dialogs now open with the same column and section layouts
345	The =VersionControl_RevNumber special string now refreshes after committing to version control.
392	Outputers with missing Data Source documents are no longer silently excluded when generating outputs. This means that errors when generating releases are detected instead of being silently ignored.

427	Floating toolbars no longer become docked after changing any setting in Preferences.
449	Fixed accidental crash during synchronizing Sch and PCB, caused by graphical parts, which have electrical sub-parts (pins). Now Graphical part is completely ignored and excluded from navigating.
453	Dialogs which were last displayed on a physical monitor that is later unplugged no longer appear outside the physical dimensions of the screen.
511	Updating a project file from version control now requires you to use the Update Whole Project command, which includes missing files by default. This makes it harder to update a project without associated added documents.
513	The Delete and Rename commands now apply to the repository as well as the local working copy.
522	Issue has been fixed through the change to doing comparisons with polygons shapes rather than file parameters.
538	The "Execution time / Abort" dialog that shows when executing long running console applications (e.g., Subversion) has been improved. It now displays the progress of the application, and a Show Details >>> section which lets you see the console output.
543	File View now has Other Documents category for unknown document types
552	A crash that occurred when pressing the Test Connection button twice, has been fixed, when using Publish To Web with an Amazon S3 destination.
563	Changing library path now only affects location of user libraries
569	A repainting issue when resizing Wizard dialogs has been fixed.
639	For Windows Vista and Windows 7 support, the NexusCache.db file is no longer opened for writing in the Program Files folder.
692	You no longer need to restart Altium Designer after changing your version control preferences.
697	Altium Designer no longer creates or depends on the file asccprj.scc when using Subversion.
717	Folder permissions are now set to avoid a problem where multiple users on a Windows Vista and Windows 7 machine can lead to Access Is Denied messages when refreshing licenses.
719	Highlighting/unhighlighting nets in Schematic document now marks the document modified
731	Performance has been improved for various workspace, file loading and closing operations in network environments.
760	File Locking is now optimized to eliminate an unnecessary file check.
784	In Preferences, when using Set To Defaults for File Types, an error no longer occurs under Windows 7 or Windows Vista.
808	The Auto Detect Subversion button in preferences now finds bundled Subversion products (e.g., CollabNet and SlikSVN) more reliably.
827	Fixed printing of images in Schematic documents in grayscale/monochrome modes.
835	Added: under Windows 7 taskbar button now shows progress status during long operations
836	Added support for the Windows 7 Taskbar: a progress bar; and for Pinning Altium Designer to add right click options for launching and for updating Recent documents.
842	Improved Spice simulation DC convergence. Dynamic GMIN and source stepping algorithms (with new options DYNAMICDC and DYNAMICDCFACTOR) are executed if initial convergence fails. Set DYNAMICDC to false to use original Spice3 convergence algorithms.
862	The Open Workspace Documents command now displays a Confirm dialog, listing a count of documents by type for you to review, before proceeding to open every document.
863	A crash, where an output is configured while the OutJob is opened as a free document, has been fixed.
871	The Open from Version Control button on the File>>Open... dialog has been replaced with an enhanced File>>Check Out... command.
872	Optimizations now allow projects using Search Paths for model libraries such as footprints to open more quickly.
877	Added bubble notification to indicate if the running build is not the latest build installed.
883	Altium Designer panels, including the Soft Instrument Racks, now correctly support the Microsoft Aero window borders, supporting Windows Vista and Windows 7 operating systems better.
913	The spelling mistake in Orcad PCB file importer has now been corrected.

920	Speed of Spice simulations containing PSpice TABLE and VALUE sources has been improved.
921	A bug in the differential of the PWR function has been fixed that existed in the original Spice3 code.
922	The LIMIT function now produces the correct simulation results when the max and min limits are not constants.
924	Alphanumeric node names starting with a digit when used in Spice simulator equations no longer cause a parsing error. And the use of undefined node names will now generate an error.
961	Annotation files for a project which are in the project folder but are not part of the project have always been used by Altium Designer. Release 10 now warns about this and will add these files into the project.
985	During parametric import of SimView waveforms, warnings are now sent to messages panel when illegal characters appear in wave names, instead of displaying dialog.
986	SimView scrollbars now update correctly after parametric import of waveforms from a file.
987	SimView waveform import now handles large files better with optimisation of imported waveforms, and ability to select via script parameters which waves to import.
1003	Interoperability between Altium Designer and MS Office 2007 and 2010 have been improved.
1009	The "Publishing to PDF" caption no longer gets stuck on the status bar.
1023	An Out of Storage error when printing or publishing Project Physical Documents of schematics containing embedded WMFs from OutJob and Smart PDF has been fixed.
1099	GDI object handles no longer leak when option to show full path in hint is off in workspace preferences
1106	A GDI object handle leak that occurred after hovering over a project icon while Project Insight is enabled has been fixed.
1111	Fixed painting of Inspector and List panels after quitting transparent state
1114	On-Demand licenses are now less likely to become invalidated by the presence of additional network adapters.
1122	Document preview files are no longer stored in the same folder as the document. Hidden sub-folder is created now to store preview files.
1251	Account Sign In - user name and password are now trimmed of leading and trailing spaces.
1260	The PADS importer will no longer create layer names longer than 256 chars when multiple PADS layers map to the same Protel layer
1306	A bug involving the positioning of ports in Convert Part to Ports has been fixed.
1371	Fixed default toolbar layout for Harness and Annotation documents
1380	Smart PDF no longer lets you generate a PDF of the Free Documents project (which would fail when creating a nonexistent directory).
1381	Schematic Parameter Sets now have a Style property. The new Bubble style is about the size of a wire junction, reducing clutter in schematics.
1382	Rotating a part with the Mirrored flag set now correctly sets the Orientation attribute, so it can be successfully used in Update from Libraries.
1383	Placing a component on schematic from the Libraries panel no longer resets the Mirror flag if you hit X or Y while dragging and the source SCHLIB file is currently open for editing.
1384	Signal harnesses with diagonal segments are now drawn correctly on the schematic document.
1453	Projects Panel Design Insight hints now use the Mouse Hover Delay preference setting, and should no longer stick to the screen.
1454	The output file or folder name in Publish To PDF settings is now saved as a relative path, making it easier to move OUTJOB files between different projects and folders.
1455	Displaying a library in the Libraries panel before any schematics are opened (so that it says Click here to draw component), uninstalling it in preferences, then clicking on Schematic preferences no longer leads to a crash.
1456	File translators will now be loaded only when the user starts the Importer Wizard.
1464	The Subversion password dialog now sticks.

1502	Project compile has been fixed to correctly group subparts together into components when assigned duplicate designators. This was causing issues with syncronisation to pcb.
1507	The Xilinx Spartan-6 board level library has been updated and now includes devices in CP196, CS484 and FG900 packages.
1532	Subversion performance has been improved in some situations involving slow network repositories.
1533	Export STEP is now available as an outputer that may be configured in OUTJOB files.
1549	.svn, _preview and history folders are not displayed anymore while refactoring a sheet symbol into a device sheet
1591	Windows Vista and Windows 7 do not allow logs to be written to the Program Files area, so the DXP.log file has been moved to the local profile, and has been renamed to portal.log.
1593	The creation of nested folders now works correctly when adding a project to a file: based Subversion repository
1612	Disruptions to On-Demand licensing caused by portal outages are reduced by increasing the time periods between lease checks.
1614	A crash when renaming project files in the Storage Manager panel has been fixed.
1620	A right click menu was added to the Class Generation page of the Project Options to allow multiple rows to be changed at the same time.
1627	The Update from PCB libraries feature has been re-engineered to fit in the new PCB Release management system
1642	Floating panels positioned on a monitor that is later detached now move to your default monitor instead of remaining off your desktop indefinitely.
1669	Fixed bug in navigation system, which caused multiple Home pages to appear
1690	Fixed F3 (Find Next) in Schematic editor
1712	The Add Project to Version Control command now pops up a browser dialog to let you select the location in the repository, and excludes files that would give you errors if you selected them.
1732	Fixed some component selection issues in the Update From Libraries dialog.
1733	Fixed issue when multiple Home pages could be opened in Altium Designer
1734	In the schematic component dialog, multiple parameters are now able to be selected.
1750	The ECO will no longer change any existing rooms when updating the PCB document with current changes. Any new components will be added without touching the room's location or position. The new components will be added in the center of the room
1756	Mapped drives are no longer absent from the SVN Browse for Folder dialog.
1789	You can now pan the 3D library PCB model preview with right click+drag. Zoom is now Ctrl+right click+drag and rotate is now Shift+right click+drag for consistency with the PCB editor.
1796	The green arrows in OUTJOB files should no longer look broken after certain operations.
1804	Text Strings can now be pasted as net objects using Paste Special
1805	A new net scope has been added to PCB projects, Strict Hierarchical. In this mode all power port objects are now local objects.
1808	Added message to the Messages Panel if project compilation finished successfully.
1809	The pin swapping dialog now shows the display mode of pins where multiple component display modes exist
1850	A bug has been fixed, where the power ports takes priority net naming option would not work sometimes when the power ports were connected to port.
1866	Enabled Document Links in components placed in device sheets
1885	The web server examples in the build now report their statistics when the address http://xxx.xxx.xxx.xxx/?action=network_stats is requested. Also the ethernet version of this example updates its MAC address to be unique based on your NanoBoard ID.
1891	Fix long startup delays when opening projects
1902	Fixed AutoBackup to not store documents if no actual modification was made since last auto-backup.
1908	There is now an Add Folder to Version Control command in the Projects and Storage Manager panels.
1922	A crash involving schematic libraries with the "Always Show Comment/Designator" option checked has been fixed.

1923	The pads that have offsets will now be exported correctly to ODB++ if they have a valid shape on solder/paste mask or silkscreen layers
1926	Designators, Comments and Parameters now update properly from the library when autoposition is off, or placed part is rotated.
1940	A redraw issue after Cutting a selection containing only pins has been fixed.
1942	Fixed Hide All in Project command
1945	Preferences are now imported page by page giving you more control over which settings you import.
1948	Fixed loosing of bus exporter/importer configuration in OpenBus after relinking the components
1975	The schematic =VersionControl_RevNumber special string should now update correctly during output.
2019	Ctrl-drag of a component no longer inserts duplicate wires where a pin connects to multiple other pins.
2020	User input is no longer processed while storing a file to local history.
2032	For improved Windows 7 compatibility, the virtualization of the file system and registry is disabled in Release 10.
2063	Live links to supplier data feature now supports Mouser.
2089	Add and Remove operations now only schedule files for addition or deletion, allowing complex changes to be committed atomically.
2091	You can now Lock and Unlock files in Subversion to avoid getting into conflicts.
2117	The Heads Up Opacity & Delay properties will now be correctly saved after changing them using the edit box controls & immediately clicking the Apply button
2123	Fixed out of memory error when Net Harnesses were connected recursively.
2142	Saving a file no longer capitalizes letters in the file name (which used to interfere with case sensitive tools like Subversion).
2147	Fixed flicking of Messages panel
2148	In Projects Panel, Close Project Documents immediately after Open Project Documents no longer causes Access Violation.
2153	Bus joiners have unique designators on a project level, instead on a document level.
2177	The Text Editor preferences now allow language to be configured even if no text document is open for editing.
2205	Special strings like "=Value" are now evaluated in parameter variations (in schematics and in outputs generated from schematic projects).
2261	When importing preferences, standard installation paths are updated to cater for software version and operating system discrepancies.
2269	Fixed occasional crash on opening workspace by drag'n'drop over opened schematic
2278	Improved GDI resource handling
2282	The Version Control menus have been made more consistent.
2283	There are now new "Resolve Conflict" and "Revert Local Modifications" commands.
2290	A crash associated with Subversion running in a directory from a disconnected drive has been fixed.
2329	Support for the MatrixOne and Microsoft SCCI version control plug-ins has been removed.
2335	Ampersands (&) are now correctly represented in the Startup/Help>>About screens.
2358	The Whole Project commands now don't hide non-project documents by default. You can select all project documents using the right click menu.
2372	Users can now select suffix options for Component clarity in their step exports
2418	Ctrl-drag of wires has been improved, redundant line segments are no longer created.
2422	Occasional crash when navigating around projects is fixed.
2423	Fixed PCB/Sch List panel when large fonts are used
2487	Added a fit to width checkbox to the Variants dialog which, when disabled will expand each column to fit to contents.
2506	Window caption of the Monte-Carlo specific tolerances dialog is no longer modified while editing grid values.

2508	Single Layer Pads on Mechanical Layers 17-32 are no longer absent from the Gerber Output.
2518	Warning message will now appear every time the user attempts to move a locked object.
2612	When running an Update from PCB libraries, the "Update from PCB Libraries - Options" dialog will contain a list of only those layers actually in use in the PCB.
2620	Net name no longer propagates between a pin designator with the same name as a net that is connected to a hidden pin.
2635	The Gerber Export of offset pads is no longer incorrect when the output layers are mirrored.
2730	Fixed resizing of Home Page
2757	Orcad DSN exporter issues causing AVs have been fixed.
2861	The error "Can't create tunnel: The system cannot find the file specified" in certain situations using svn+ssh: repositories has been fixed.
2880	Make PCB Library no longer intermittently causes pad size changes.
3082	P-CAD ASCII Export will now write the "CompPinRef" fields in ascending order taking into account if the pad names are numerical or not. This will insure that the order for numerical pad names will be 1, 2,3 ..10, 11,..20, 21 and so on.
3153	Supplier Link fields in a BOM can now be sorted properly without causing an error message.
3169	The PADS Importer now is able to load PADS ASCII files V2005.2 that contain a DOCUMENTS_LIST section before the PADS LAYERS section.
3176	ODB++ output will no longer discard fills that are rotated 360deg instead of 0deg.
3178	The ECO from Schematic to PCB will no longer place some multi-channel components in the middle of the whole PCB workspace (~1.2m away).
3181	The Specctra Design Files now import as expected.
3310	When saving PcbDoc in DXF/DWG format, rounded rectangle pad shapes are now exported correctly.
3420	An "Out of Memory" exception will no longer occur when generating ODB++ for designs containing No Net hatched copper-pours on any of the signal layers.
3511	ODB++ output of attributes has been improved. Now following attributes will no longer be exported:.connector, .target, .component, comment, hole_type, gold_finger & serial_number.
3856	A new context sensitive search feature is added to the DXP menu allowing searches of live compiled project data such as Reference Designators, menu commands and other product information.
3857	Varied project parameters will now display correctly in PCB & also in assembly, Gerber & ODB++ outputs.
4144	A large delay is no longer experienced when opening a schematic when the "Write debug information into the Output Panel" preference is enabled.
4181	Issue when commit releases that contains no Schematics document, that causes release to fail.
4290	Synchronize sheet entries and ports now works correctly.
4306	The number of installed plugins is now consistent, it always includes the base platform module.
4362	Strings such as "Tolerance" now evaluate correctly in Schematic special Strings.

FPGA and Embedded

38	Fixed bug in Terminal instrument, which causing embedded application to stuck unless Terminal window is opened
85	The USB symbol of the FPGA NB3000 Port-Plugin library has been reviewed and the USB_D port corrected to USB_D7..0 as expected.
97	Additional line feed are no longer issued to the output panel after stepping over printf function calls while debugging code.
115	Menus of the lab feature AGUI editor have been reviewed and are no longer docked to the wrong side of the workspace.
126	The FPGA IP Import Wizard has been reviewed and is now able to import complex Altera cores with encrypted source files.
128	The SDRAM controller has been improved for speed and is now offering caching capabilities.

129	Added scripting support for Wishbone Probe instrument.
131	Wishbone Probe can now be used on the peripheral side of the processor
132	Certain errors in FPGA projects have been escalated to Fatal Errors, to ensure the build flow is stopped as early as possible when serious errors are found.
134	Added scripting support for Crosspoint Switch instrument.
137	A new option has been added for the Devices View to automatically save FPGA source documents before running the flow.
138	New WB_CELLULAR and WB_GPS_NMEA cores have been added with Software Platform drivers for implementing GSM (2G/3G) and GPS applications. Example projects can be found in the "Examples\Soft Designs\Mobile" folder.
141	Re-compiling FPGA projects is no longer causing FPGA and Embedded projects to be marked as dirty if they haven't been modified.
152	A new reference design illustrating how to use the support for USB WiFi is now available in the Examples\Soft Designs\Showcases\NB3000 USB WiFi MSD Webserver directory.
157	It's possible now to use in OpenBus external memories and peripherals (via bus exporters)
161	The configurable clock manager component now supports Actel ProASIC, Fusion and IGLOO devices.
201	The Synthesize command from the Design menu for FPGA project is no longer failing to find pre-synthesized models for some configurable components - including the WB_SPI core.
228	The size of the internal memory for 32-bit soft processors is no longer limited to a size of power of 2 and it can now be set to any values.
243	The memory size for the flash memory controller of the NB3000 Shared Memory Controller is now set to 16MB to reflect the size of the parallel flash memory device fitted on the NB3000.
283	Renaming a processor on an OpenBus sheet no longer removes interrupts connected to that processor.
293	The FPGA_STARTUP components have been reviewed to fix incorrect number of delay cycles while targeting some devices - including Spartan-3AN, Spartan-6, Virtex-4 and Virtex-6 devices.
303	A new WB_MP3DEC core with Software Platform drivers is now available and a reference design to illustrate why to use it is available in the Examples\Soft Designs\Audio\NB3000 MP3 Decoder folder of the installation of Altium Designer.
375	The TFT_PEN symbol of the FPGA NB3000 Port-Plugin library has been reviewed and its pins re-ordered to make connectivity with generated harness connectors of SPI cores easier.
383	High CPU utilization as well as some minor performance issues have been addressed in USB JTAG implementation
385	Software Platform documents no longer appear empty if opened as a free document.
430	The Software Services section of the Software Platform document has been review and services links and names have been updated for clarity and constancy.
432	The choice of HDL to use can now be set at a project level, for synthesis and for simulation. These settings are available in the project options and will default to your global preference under general FPGA preferences.
452	Processor now remains paused in a debug session when the PC register is changed using the Nexus Debugger
493	A new reference design illustrating how to use the Plug and Play support for USB Webcams is now available in the Examples\Soft Designs\Display\NB3000 USB Video directory.
497	The serial and parallel flash memory programmers are now available for the NiosII processors.
498	Software platform startup code (in cstart.asm) can now be placed in external memory.
528	Expanding large arrays no longer causes AD to crash
585	The WB_SPI8, WB_SPI32 and WB_SDCARD cores can now be used together on the same design without causing Build errors while targeting an Altera device.
586	Nios compiler error for inline assembly with "m" constraint has been fixed.
629	Added item to messages view when embedded project files are downloaded
686	The "Select Processor" entry can now be changed only for "Generic" TASKING devices. The entry is fixed (disabled) for all other device selections.

688	A software platform problem on NiosII with thread context switching and native interrupts has been fixed.
699	The configurable clock manager component now supports Spartan-6 devices.
702	Adding multiple NiosII processors in a schematic based FPGA project is no longer causing the FPGA flow to fail.
713	An error "Unable to find child model Configurable_UX in output folder" is no longer issued when trying to publish a core project that includes generic configurable components.
739	AltiumSynthesizer does not infer circuits for divide and modulo operations. An error is issued when a div or mod operator is used in the HDL.
748	The constraints files for the NB3000XN board have been updated to avoid an error in the FPGA flow while timing requirements have been set to the ETH_TXC and ETH_RXC ports of the Ethernet interface.
758	Fixed a problem where debugger could enter an infinite loop when updating variables.
765	Double clicking on Linker error in the Messages panel no longer opens Embedded Project file.
769	If attribute FPGA_INHIBIT_BUFFER is associated with an object then attribute FPGA_IOSTANDARD is neglected (i.e. not passed to SIS/Map not passed to edif).
794	Message Panel now shows correct format if source file path contains parentheses.
796	The Software Platform library is no longer recompiled unnecessarily when the Embedded project is unmodified.
797	Running an ARM application in the instruction set imulator no longer fails for ARMv6M and ARMv7M Cortex cores.
824	The WB_SPDIF core no longer generates spurious interrupts.
851	It is now possible to add signals to the Logic Analyzer and Digital IO instruments using the Paste button of their configure dialog while objects like NetLabels have been copied using Ctrl+C - Copy As Text is no longer required for this operation.
886	Sections in AltiumSynthesizer report files can be collapsed/expanded facilitating easier navigation within the file.
903	FPGA Configurable Generic IntLib extended with Divider/Modulo and Multiplier components.
923	Actel Igloo Nano AGLN010 device is now supported
930	It is now possible to set pin to pin, pin to flipflop and flipflop to pin maximal timing delay in the Constraints editor using the FPGA_DELAY_MAX, FPGA_DELAY_MAX_FROM and FPGA_DELAY_MAX_TO constraints.
974	Windows computer waking from sleep while connected to running NB3000 does not cause problems in AD scanning jtag.
1011	In System Flash support for Spartan3AN devices has been improved. Only sectors required for programming device are erased during operation preserving user data.
1041	The Miscellaneous Import The Following Data Object Files Linker option for Embedded project is now adding imported objects to the dependency list of the generated makefile as expected.
1042	Support for C library 'errno' has been made thread safe in Software Plaform Multithreading Support.
1051	Compile mask for code symbols can be applied without side effects on code symbols that refer to the same C source file.
1058	It is now possible to change the default initialization of memory components from big to little endian via a new option in the configurable memory component dialog or by adding an endianness parameter with a value set to little for memory components of the FPGA Memories library.
1097	The configurable clock manager is now working as expected while targeting a Xilinx Spartan-3E Automotive device.
1102	CHC log files are added to project; Individual functions are outlined; Variables and functions are color coded.
1116	Core projects targeting Altera devices can be synthesized with Altium Synthesizer now. Duplicate component error from Quartus when both main design and core projects were synthesized with Altium synthesizer are resolved now.
1119	The Terminal instrument has been improved so that it will not cause the controlling processor to hang. Previously the processor would hang if the terminal was visible and then shut down, or the JTAG connection lost. This no longer happens.
1120	Software Platform Multithreading Support now includes support for Semaphores. Check knowledge center for API description.
1153	The Fit Document command in the View menu of the waveform editor no longer shows the simulation signals up to the time of the last transition that occurred, but instead shows signals up to the time the simulation has been ran to.
1194	It is now possible to create Verilog libraries for FPGA and Core projects.

1196	It is now possible to generate Verilog testbench files automatically from Schematic and Verilog files through the Create Verilog Testbench command of the Tools Convert menus.
1204	It is now possible to generate Adder/Subtractor components from the FPGA Generic Library in Verilog format.
1206	It is now possible to generate Joiner/Splitter components from the FPGA Generic Library in Verilog format.
1207	It is now possible to generate Comparator components from the FPGA Generic Library in Verilog format.
1209	The MUX and DEMUX components from the FPGA Configurable Generic Integrated Library can now be generated in Verilog format.
1210	It is now possible to generate PWM components from the FPGA Generic Library in Verilog format.
1211	The Register Component from the FPGA Configurable Generic Integrated Library can now be generated in Verilog format.
1214	Pre-compiled libraries for Vendor specific resources are now included by default while running HDL simulations and can be managed through the FPGA Simulation Compiler system options.
1215	It is now possible to Highlight and Reverse Bus signals during HDL simulation.
1220	The simulator is now properly starting with the selected testbench when multiple testbench files are included in the project.
1221	Simulation Testbench Document option for FPGA project is now properly saved when testbench files with same names but different extensions are included in the project.
1223	The Compile command is no longer missing in the Project menu and the Right Mouse click menu of the Projects Panel when a VHDL or Verilog testbench file in focused.
1258	TCP/IP stability is improved
1268	New CodeSymbol Explained reference designs for NB2 and NB3000 are available in the Examples\Soft Designs\C to Hardware\ folder of the installation of Altium Designer which illustrate all "interface types" supported by C Code Symbols.
1272	All generated files for HDL Simulation are now generated in a single output folder to avoid conflicts.
1309	Software Platform support for multiple interrupt handlers per interrupt line.
1310	EMAC32 driver support for rx/tx interrupt notification.
1311	UART8 driver supports non-blocking mode and several blocking modes for threaded applications.
1314	Software debugger now does a hard reset instead of a soft reset when starting the application.
1319	Fixed an issue where swplatform.h sometimes failed to include certain plugin-generated headers.
1325	An error is now reported for c to hardware code symbols when there is a mismatch between c parameters and code entries.
1360	An error "Unable to find Synplicity For Actel" no longer occurs while the synthesizer is set to Synplicity For Actel and Actel Libero 9 is installed.
1362	CHC Wishbone Multi-Cycle Bus Adapter asserts DONE signal after reset. This enables you to test whether a hardware function is active before calling that function.
1438	The pins of rotated and mirrored configurable components are now placed and aligned as expected after the component is re-configured.
1439	An access violation in verapi.dll no longer occur when Verilog source files contain synthesis attributes - including the synthesis syn_ramstyle attribute.
1442	Collision when processor connected to Terminal instrument and Altium Designer Nexus driver try to update the Terminal instrument status register at the same time, causing characters to be incorrectly captured in instrument rack panel, no longer occur.
1443	The synthesis stage of the FPGA flow no longer fails while NANOBOARD_INTERFACE instruments are included without a connected script project.
1444	The AB_SYSTEM component is no longer missing from the Actel Fusion FPGA library.
1445	Configurable Memory Instrument no longer fail the FPGA build flow when the Support Byte Enable option is selected.
1446	Pressing the Space key no allows to toggle between different shapes (normalized, flipped, straight) while placing links in OpenBus document.
1447	Added scripting support for Frequency Counter instrument.

1448	Added scripting support for Frequency Generator instrument.
1449	Added scripting support to Terminal instrument.
1450	Names of black box modules referenced in Verilog had been rendered incorrectly under certain circumstances. This has been corrected.
1451	External tristate buffers are no longer instantiated incorrectly for internal ports.
1452	The synthesizer now emits a warning if an output signal is used in a sensitivity list.
1461	The C++ project option "Check for Embedded C++ compliance" is changed into "Comply to embedded C++ subset". The explanation is improved.
1470	Endianess problems with support for Altera's little-endian Nios II processor core have been resolved.
1477	An issue with the flipflop optimization of the Altium synthesizer has been corrected.
1488	Synthesis of configurable digital IO no longer fails with XST when schematic netlister is verilog.
1499	Generic ClockManager - Fixed "No Solution " being shown when no device is present in devices view.
1506	The Xilinx Spartan-6 driver has been updated and now includes devices in CP196, CS484 and FG900 packages.
1508	Shared Memory Controller includes Wishbone bus arbitration logic now allowing other multimasters to be wired directly to its ports bypassing wishbone interconnect.
1511	The Create HDL Testbench commands have been moved from the Tools Convert menus to the Simulator menu.
1536	C compilers in Altium Designer now support the CERT C Secure Coding Standard as defined by CERT (www.cert.org).
1550	AltiumSynthesizer: Portnames of a VHDL entity instantiated within a Verilog module are mapped case insensitive when a case sensitive attempt fails.
1603	It is now possible to set multiple testbench configurations for a project and the configurations can be selected directly from the Simulator Simulate submenu.
1607	Warnings about duplicated constraints are no longer issued during Translate Design while targeting a Xilinx FPGA.
1611	NB3000 firmware has been improved. Clock settings are correctly saved on change.
1617	No longer need to call CreateSignalInstrumentManager and ReleaseSignalInstrumentManager to be able to use Digital IO instrument from scripts
1628	i2cm_open now times out if no I2C slave is connected and no longer causes the application to hang
1675	Support for distributed memory for Lattice FPGAs has been added in Altium Synthesizer.
1686	Color coding of C language extensions used by C Code Symbols has been implemented.
1729	POSIX kernel signal queue no longer corrupted if last member gets re-inserted.
1730	Stacks are initialized with a non-zero byte pattern when Multithreading Support DEBUG option is set.
1739	MIDI Software Platform peripheral plugin has been updated to distinguish it from other UART8 plugins.
1781	The Lightweight IP TCP/IP stack included with the Software Platform has been updated to version 1.3.2.
1853	Programming Altera FPGAs via JTAG is no longer failing while the On-Chip Bitstream Compression project option is enabled.
1854	Context restore from POSIX interrupt on TSK3000 now properly restores IEp bit.
1865	Reference/Dereference is removed from Code Formatting, Spacing in embedded project options.
1869	OpenBus bus importer and exporter pins can now be included or excluded individually.
1887	When a configurable REGISTER from the FPGA Configurable Generic library is configured as type Transparent Latch its logical behavior is was not correct. This issue is now fixed and correct behavior can be expected.
1890	Empty string attributes in vhdl are correctly translated in Altium Synthesizer produced edifs.
1913	Removed inconsistent "drv_" prefix from TMR3 driver API in software platform.
1920	For inferred RAM: if the size of the array in not equal to the size that can be decoded with the address lines then an informational message is displayed. Example: WARNING: BLOCK RAM 'ram' address bit #0 is constant (net "(VCC)").

2008	PB01 VIDIN_PCLK video input clock is constrained in the PB01 constraint file now. Maximum frequency is set to 27MHz.
2052	Added two new predefined macro's _ALTIUM_BUILD_MAJOR_ and _ALTIUM_BUILD_MINOR_ containing the build numbers for Altium Designer and useful to create conditional C code.
2058	Posix function sigwaitinfo() now returns the selected signal number or -1 to indicate an error.
2155	EvalBoardTester Design has been modified. Bus constants have correct format modifiers now.
2166	Nios interrupt handler is now always installed when software timers are switched on in Software Timing Management service.
2178	Preferences for text editors now allowed to select any custom color for syntax highlighting.
2211	tvp5150_get_register function in software platform returns correct value now.
2233	Programming Lattice ECP2 devices configured to boot from external SPI via JTAG no longer failed to program when the SPI device is programmed.
2240	SwPlatform file can now be moved around in sources list of project panel.
2375	Order of the RGB leds are no longer reversed when using the LEDS_RGB port plug-in for NB3000AL board.
2388	Scaled print from waveform viewer now looks correct
2399	Resolved issue where LED controller cannot be set to "Signal Harness" interface type.
2403	Embedded project compile now benefits from multicore host machine to speed-up compilations.
2426	VHDL Libraries are now working as expected while set for Synthesis.
2433	POSIX kernel routines for attribute initialization will now re-initialize argument object when invoked more than once.
2465	Editing Openbus component Interconnect before placement no longer causes Altium Designer to crash.
2474	Order of the DIP switches as shown on the board silkscreen are no longer reversed when using the DIPSWITCH port plug-in for NB3000AL board.
2530	Altium Designer no longer crashes at synthesis when using NiosII in the FPGA projects.
2541	Altera QuartusII and Nios10.0 is now supported in Altium Designer.
2543	Xilinx ISE12.2 is now supported in Altium Designer.
2663	Improved typedef resolving for proper typename lookup.
2668	Provide a more meaningful error message if software platform is not found.
2718	DualMaster and Multimater arbiters have been improved. Address bus width 1 is correctly handled in schematic and Openbus designs.
2767	Programming Actel ProASIC+ devices while running a computer that does not have a parallel port no longer causes series of crashes.
2810	SPB inspector description pane now shows a scrollbar when the text does not fit
2819	Changing the options MQ_OPEN_MAX and MQ_PRIO_MAX for the "Message Queues" service have no effect.
2829	NB3000 Firmware update procedure has been improved. Erase/Programming flash device status is handled correctly now.
2836	Peripheral base addresses and interrupt numbers are now available as macros through automatically generated software platform "devices.h" file.
2838	In an embedded ARM project it is now possible to set the Thumb code generation option separately for each individual C/C++ module.
2854	Threads panel now shows correct scheduling policy for threads with a scheduling policy other than FIFO.
2855	Support for "->" and "::" as field separators was added
2894	EMAC32 core has been improved. The core automatically reports link status changes via interrupt mechanism.
2898	C compiler now supports anonymous unions in structure definitions.
2917	Out-of-memory condition in pthread_setspecific() no longer results in NULL pointer access.
2925	Expanded variables are now shown expanded after target execution

2929	Maximum POSIX thread stack size in the software platform is no longer limited to 64kB.
2953	Memory Controller MEM_CTRL has been improved. Generated HDL code for Asynch memories no longer produces a warning during build process.
2971	GUI example is updated with interrupt connected and it now runs on NB2 per configuration.
3030	DualMaster and Multimaster components have been improved. They no longer produce warnings during synthesis stage.
3047	Altera Cyclone 3 default IO Standard Voltage setting has been adjusted to 2.5V.
3053	POSIX sporadic server thread now frees its timers upon thread exit.
3068	A return code bug in CAN driver can_getdata_rxmo() is now fixed.
3073	The Debugger Timeout dialog has been review to focus controls in a more conventional order when pressing the arrows keys.
3101	FPGA Signal Manager has been improved. Assign Unconstrained Signals function operates correctly on ports with long names.
3133	Spartan3AN In System Flash support has been improved. Programming internal flash works correctly regardless of FPGA position on jtag chain.
3146	NB3000 Slideshow example update for NB3000 boards. SPI Flash start address has been corrected for each NB3000 target.
3170	Configurable Clock Manager has been improved for Altera targets.
3183	UCF file import no longer crashes with missing ";".
3203	Fixed ARM simulator to handle interrupts also correctly in Thumb2 (Cortex M3) mode.
3235	The Place and Route stage of the FPGA flow no longer fails with an error "The PAR option, "-t" (Starting Placer Cost Table), is disabled for this architecture" while targeting a Xilinx Virtex-5 and Virtex-6 device and ISE 12.x is running.
3372	Xilinx UCF files are now imported as expected when the Construct Bus Constraints option has been enabled.
3427	Corrected the default value for USB JTag Speed slider in the FPGA Preferences panel.
3660	Altera QuartusII and NiosII version 10.1 are now supported.
3674	Module ports expressed in Verilog 2001 style where not listed in CodeExplorer, this is fixed.
3860	Posix ASR context switch routine has been updated to handle tsk3000 previous interrupt enable flag.
4010	The Xilinx CoolRunner XPLA3 devices with PQ208 package are now properly recognized in the Devices View.
4272	Programming Actel devices when running Windows-7 is no longer failing.

Altium Designer 10 Update 1 (Platform Build 10.467.22184) – March 24, 2011

System Components: PCB System

4199	'Delete all grids and guides' in PCB Libraries now marks the file as Altered.
4313	An access violation will no longer occur in PCB Preferences / DRC Violations Display page when trying to set Violation details for Used rules only when no PCB document is open.
4386	An access violation will no longer occur in PCB Differential Pairs Navigator when Mask/Dim is used & there are differential pairs with invalid (null) positive / negative nets.
4460	Enhanced clearance rule to support differential pair checks and fixed bug when clearance was not applied on objects in the same diff pair. *More info*. *View BugCrunch report*.
4546	Max/Min Width Rule no longer creates bogus violations on InternalPlanes.

System Components: Schematic System

3513	Unicode strings are no longer truncated when saving schematic files.

Altium Designer 10 Update 2 (Platform Build 10.494.22274) – April 12, 2011

System Components: Altium Designer Base

3037	The full component update option can be set to maintain parameter positions or move them to default positions. *View BugCrunch report*.
4114	Schematic Library report images will now be correctly sized.
4382	The Help menu "What's new in Altium Designer" link to the New Features page of the wiki has been updated.
4413	Links to forum in the DXP and Help menus have been updated to point to AltiumLive forums.
4506	The drop down button in Update from PCB Libraries will now run the function displayed on the button. *View BugCrunch report*.
4513	The ECO dialog will display a warning if there were any compilation errors when creating the ECO.
4548	DXPProcess URL protocol is registered to install plugins and updates from the Internet.
4662	Flags in DXP.exe have been set to enable access to 4GB of address space on Win64 based systems.

System Components: Altium Designer Installation System

4275	Create Installation Repository tool can now include standard installation packages so that the end user can select standard options during installation.
4548	DXPProcess URL protocol is registered to install plugins and updates from the Internet.
4562	AltiumInstaller no longer prompts to sign in if the repository is local.

System Components: Schematic System

4114	Schematic Library report images will now be correctly sized.
4558	An error that can appear after selecting and editing schematic library Designators and Comments has been rectified.
4621	Changing the default mode on a component from the tools menu will set the modified flag on a SchLib file as happens when you edit the component.
4733	Fixed infinite loop when updater cannot start from non-admin user account.

Hardware Support Packages: Device Support - Xilinx Spartan-3AN

4580	Programming, erasing and verifying the In System Flash of Xilinx Spartan-3AN devices is no longer failing.

Altium Designer 10 Update 3 (Platform Build 10.516.22330) – April 29, 2011

System Components: Altium Designer System

1997	An Access Violation that used to happen when switching between PCB & SCH documents after doing a SCH to PCB ECO followed by PCB Interactive Routing with Pin Swap ON has now been fixed.
Various	The following preferences can now be exported and imported: System > Transparency System > Navigation System > Design Insight System > File Types* Data Managem ent > Backup Data Managem ent > File Locking* Data Managem ent > Local History* Data Managem ent > SVN Libraries* Scripting System > Global Projects* Scripting System > Form Designer * Remains excluded from Cloud Preferences.
4774	Altium Designer in some cases displayed Catastrophic Failure messages and is now improved to display the correct exception dialog.

System Components: PCB Support

Various	The following preferences can now be exported and imported: CAM Editor > General CAM Editor > View/Language CAM Editor > DRC CAM Editor > Import/Export CAM Editor > Miscellaneous CAM Editor > Drawing Modes CAM Editor > Film Box CAM Editor > Draw Dimension
4571	CAMtastic® Reload layer data command no longer unexpectedly shuts down Altium Designer. *View BugCrunch report*.

System Components: Schematic System

2577	The preferences in page Schematic > Orcad can now be exported and imported.
4666	Schematics now display text correctly in all supported languages and simulations work correctly regardless of the machines language settings. *View BugCrunch report*.
4775	The Schematic update from libraries, Preserve parameter locations option, will no longer update the component's parameter with the Autoposition setting from the library component's parameter.

System Components: Schematic Support

2596	The preferences in page Simulation > SIMetrix Interface can now be exported and imported. Remains excluded from Cloud Preferences.

System Components: Soft Design System

Various	The following preferences can now be exported and imported: FPGA > NanoBoard Firmware Updates Embedded System > General Embedded System > Libraries* Embedded System > Code Formatting, General Embedded System > Code Formatting, Spacing * Remains excluded from Cloud Preferences.
4371	Access violation no longer occurs when there is no profiling result available.
4436	Embedded code editor no longer freezes some time when some codes are highlighted.

System Components: Soft Design Support

4518	Underline typing errors in Editor preference no longer causes Altium Designer to crash

System Components: Soft Design Firmware

2988	Version 1.0.26 of the NB3000 firmware is now available. *See Firmware release notes*.

Output Generators: Output - Gerber

4346	Gerber Output will no longer contain layers that were removed from the PCB board layer

Output Generators: Output - Testpoint

4559	The TestPoint Report (IPC-D-356A netlist) no longer creates incorrect output when buried vias are present.

Altium Designer 10 Update 4 (Platform Build 10.537.22385) – May 13, 2011

System Components: PCB System

3648	Import of board outline boundaries containing arcs and multi-line component Description text has been corrected.
4397	PCB will no longer cause AD to run Out of Mem ory when changing one or more properties of component designator/comment using the PCB Inspector for large boards with components containing 3D bodies.
4467	The Long delay / GUI lock-ups after long PCB operations requiring a lot of Undo compressions no longer happens.
4595	"Duplicate Rule" menu item has been added to the right click menu in the "PCB Rules and Constraints Editor". Duplicate rule is given the next priority down from the rule being duplicated. *View BugCrunch report*.
4649	DRC Clearance Violations now show the actual distance compared to the rule distance in the text summary. *View BugCrunch report*.
4725	Coordinate "Text Height" property can now be edited when using the PCB Inspector / List panels. *View BugCrunch report*.
4759	A typo was fixed in the Confirm dialog shown when defining a board shape from a STEP model and a non-planar face was selected.
4838	A crash on closing a PCB document if copper pours are modified & then rem oved from the design will no longer occur.

System Components: Schematic System

4592	A four-way junction formed in a schematic will no longer be replaced by a cross over by the optimizer. *View BugCrunch report*.
4870	Four-way junctions are no longer optimized out of schematics. *View BugCrunch report*.

System Components: Data Management

3999	An error no longer occurs when pasting from an Excel spreadsheet back into the Component Definitions region of a Component Library file.
4050	The Download command on the right-click menu for a vault component has been removed.
4250	The detailed Item view for a vault-based Item will now always be brought into focus when using the "Full Item Details" command.
4251	You can now view the lifecycle diagram for items in the vaults panel and also establish new revisions from there.
4278	It is now possible to change the case of a parameter name in the Component Library Document.
4347	PCB Component and SCH Symbol cannot be placed from the vaults panel. Placement is done with Components. The menu commands are now hidden to avoid confusion.
4847	Download component will create a folder with release documents for both symbol and footprint now.
4895	When connecting to a vault, using alternative credentials are now unchecked by default.

System Components: Altium Designer Localization

4766	Japanese localization of Altium Designer updated.
4832	Korean localization of Altium Designer updated.
4833	Simplified Chinese localization of Altium Designer updated.

Altium Designer 10 Update 5 (Platform Build 10.545.22410) – May 19, 2011

System Components: Altium Designer Base

4616	Now UNC paths will be able to be used when generating ODB++ outputs.
4905	An Access Violation with message "Access Violation "View-1687783792" is not a valid component name at **address*" when trying to select components from the Navigator Panel for very large design will no longer occur.

System Components: PCB System

4494	Flipping a component during move no longer loses the ref point. *View BugCrunch report*.
4597	The actual height of a component that has a 3D body with a non-zero OffsetHeight is now calculated correctly for DRC. *View BugCrunch report*.
4717	Changing Mechanical Layer Pairs assignments (add, remove, update Mechanical Layer Pairs) will now mark the PCB Document as Modified.
4738	The "PCB Hole Size Editor" no longer creates multiple entries for the same hole size when old slot hole length is retained after changing the hole type to Round.
4905	An Access Violation with message "Access Violation "View-1687783792" is not a valid component name at **address*" when trying to select components from the Navigator Panel for very large design will no longer occur.

System Components: PCB Support

2813	IBIS converter tool now supports Model Selector keyword and allows selection of the model within the signal integrity model dialog. *View BugCrunch report*.
3252	An issue preventing reflection results from being generated for some designs due to generation of a long combined net name has been fixed.
4401	A problem with the list of sch pin in the SI Part Array dialog has been fixed.
4465	CAMtastic® Gerber Export will no longer create Gerber files that can't be loaded back into CAMtastic® correctly when using RS274X format & Incremental coordinate data.
4497	CAMtastic® ODB++ import for embedded board arrays will no longer reset the drill layer pairs for some of the child boards if any of the arrays is mirrored.
4577	Allegro Gerber files containing nested polygons will now load correctly in CAMtastic®.
4581	CAMtastic® "One or More Layer Types are duplicated/not defined!" information dialogue will no longer be stuck in an infinite loop if the user clicks the "No" button.
4619	CAMtastic® Gerber loader will no longer discard OrCAD Gerber files that use M2* command instead of M02* for marking the end of the file.

System Components: Schematic System

4481	After pasting a component to the Sch Library panel, the component will now be selected and focused. *View BugCrunch report*.
4587	Shift click now enters inplace edit of selected text object when Shift Click to Select preference is enabled. *View BugCrunch report*.
4905	An Access Violation with message "Access Violation "View-1687783792" is not a valid component name at **address*" when trying to select components from the Navigator Panel for very large design will no longer occur.

System Components: Soft Design System

1377	The Messages panel now opens on HDL simulation error.
1479	Cross probing in the Messages panel is now supported when running HDL simulation with the Aldec OEM simulator.
3063	Actel Libero/Designer 9.1 is now supported.
4922	Timing constraints are now properly passed to Actel Designer while using Synplify or Synplify For Actel.
4923	Rebuilding a project in the Devices View is now waiting for Synplify For Actel to be closed in order to avoid missing or corrupted files to be processed by Actel Designer.
4928	The FPGA_DELAY_MAX, FPGA_DELAY_MAX_FROM and FPGA_DELAY_MAX_TO constraints are no longer set with incorrect values for bus signals.

System Components: Soft Design Support

3501	Some components from the FPGA Configurable Generic and the FPGA Instruments libraries (including FIFO and LAX) are no longer failing while using Synplify or Synplify for Actel.

System Components: Soft Design Synthesis Libraries

4632	Some components from the FPGA Generic library are no longer causing the FPGA flow to fail because they have the same name as an Actel Macro while targeting Actel IGLOO devices.

Hardware Support Packages: Device Support - Actel IGLOO nano

3315	FPGA flow is no longer failing because of missing pre-synthesized modules for components from the FPGA Generic library while targeting an Actel IGLOO nano device.

Output Generators: Output - ODB

4835	ODB++ Output will now export Signal Layer Polygon Regions to corresponding ODB++ nets in case they are part of any PCB nets. *View BugCrunch report*.

Altium Designer 10 Update 6 (Platform Build 10.554.22457) – May 26, 2011

System Components: Altium Designer Base

4886	Column widths are now restored correctly in the browse for component dialog. *View BugCrunch report*.

System Components: PCB System

4957	An Access Violation that used to occur while nesting multiple Paste Text commands has now been fixed.
4985	The actual distance displayed for DRC Clearance Violations has been fixed in cases where erroneous values such as "6.254mil < 0.004mil" and "0 mil < 62 mil" were reported
4987	An error in the PcbDoc STEP exporter has been resolved, whereby 3D bodies would be exported at an incorrect rotation.
4995	Clearance Rule no longer incorrectly reports collision between two Rounded Rectangle Pads.

System Components: PCB Support

4845	CAMtastic® will now generate correct outlines for rounded rectangular pads when using the "Analysis / Generate Outlines" command. *View BugCrunch report*.

System Components: Soft Design System

1356	The FPGA flow is no longer failing because of conflicting Pull Up/Down and IO Standard constraints while targeting an Actel device.
4907	Altera Quartus2 and Nios2 v11.0 are now supported.
4920	Flow Status in JTAG chain is correctly refreshed when device is removed in offline mode.
4924	IO Standard constraints are now passed to Actel Designer as expected when using the Synplify or Synplify For Actel synthesizer.
4971	Waveform editor integration with Aldec OEM simulator has been improved. Waveform is correctly displaying all events from simulator.

System Components: Soft Design Support

1356	The FPGA flow is no longer failing because of conflicting Pull Up/Down and IO Standard constraints while targeting an Actel device.

System Components: Data Management

5001	Painting the hot highlight rectangle in the Vault Explorer search results view has been fixed so that it is no longer sticky.
5002	Searching in the Vault Explorer no longer crashes in Windows XP.

System Components: Device Registry

4947	Altera Cyclone-4E devices are now recognized in the Devices View as expected.

System Components: Altium Designer Localization

4919	Simplified Chinese localization of Altium Designer updated.
4940	Korean localization of Altium Designer updated.
4943	Japanese localization of Altium Designer updated.
4982	Traditional Chinese localization of Altium Designer updated.
4999	Shortcuts in the Japanese menu are no longer duplicated.

FPGA Components: FPGA Configurable - Generic Logic

4726	Configurable Counter Component has been improved. Output declared as individual pins is handled correctly.

Hardware Support Packages: Device Support - Altera Cyclone 4E

4947	Altera Cyclone-4E devices are now recognized in the Devices View as expected.

Hardware Support Packages: Device Support - Xilinx XC9500

4543	The FPGA to PCB project wizard is now finding Xilinx XC9500 and XC9500XV devices as expected when the corresponding board level libraries are installed.

Hardware Support Packages: Device Support - Xilinx XC9500XV

4543	The FPGA to PCB project wizard is now finding Xilinx XC9500 and XC9500XV devices as expected when the corresponding board level libraries are installed.

Importers and Exporters: Exporter – Ansoft

4635	Some Ansoft Exporter issues have been fixed. ID_ has been removed from CompInst IDs, problem characters in names and netnames are replaced, and a problem with flipped and rotated footprints has been fixed.
5021	An access violation in the Ansoft Exporter has been fixed.

Importers and Exporters: Importer – PADS

3484	Schematic library part and CAE decal files (*.p and *.c file couples) are now imported into Altium Designer more reliably.
3648	Import of board outline boundaries containing arcs and multi-line component Description text has been corrected.
3967	Support of V2007.0 and V9 Schematic and PCB Designs, and Schematic and PCB libraries has been added.
4247	PCB ascii file text widths and slotted hole orientations have been corrected. Invisible signal layer Part Type attributes are suppressed.
4415	Import of PCB circular keepouts as rooms now produces correct room boundary and places the room on the proper layer.
4525	Import of Schematic libraries has been improved when decal definitions in the CAE decal file (*.c) are missing optional fontInfo fields.
4824	Import of keepouts as rooms now produce proper room boundaries when the keepout boundary contains arcs.

Altium Designer 10 Update 7 (Platform Build 10.564.22479) – June 1, 2011

System Components: Altium Designer Base

4383	The Configuration Memory tab, part of the Options for Embedded Project dialog, is updated correctly when the Device is set for the first time.
4484	Edit PCB Rule from schematic directive - added combo box for user to choose PCB stack to see width values resulting from impedance settings. View BugCrunch report #107. View BugCrunch report #204.
4625	When Cortex M architecture (ARMv6M and ARMv7M) is selected in embedded project option, it now correctly shows no secondary stack in Locate option.
4721	Opening and closing the Options for Embedded Project dialog is no longer causing a memory leak.
4826	Parameters and Device Sheets tabs are removed from embedded project options since they are not used.

System Components: PCB System

4761	Placing blind/buried vias in a PCB Library Editor will no longer cause crashes if the PCB Footprint Viewer is in 3D mode.
5028	An Access Violation while dragging multiple tracks (more then 12) in PCB Editor will no longer happen.

5050	PCB Silkscreen Over Component Pads Constraint will no longer generate false positive violations.
5061	Displayed DRC Clearance Rule violation value will no longer be wrong when rectangular, octagonal or rounded rectangular pads are in violation.

System Components: Schematic System

4484	Edit PCB Rule from schematic directive - added combo box for user to choose PCB stack to see width values resulting from impedance settings. View BugCrunch report #107. View BugCrunch report #204.
5034	Fixed random crash when you try to save ddb library in schematic or publish schlib.

System Components: Soft Design System

4370	Cancel embedded project options no longer stores a modified device.
4392	Manipulating the Cross References panel while it is empty no longer causes an AV to occur.
4721	Opening and closing the Options for Embedded Project dialog is no longer causing a memory leak.
4746	Device selection in embedded project now handles the arrow and enter keys correctly.
4909	Embedded Document Options have no effect on intermediate files.

System Components: Data Management

5036	A crash and drawing issues in the Vault Explorer search results list have been corrected.

FPGA Components: FPGA Configurable - Custom Wishbone Device

4584	The channel count macro for WB_INTERFACE components, generated as part of the software platform (wb_interface.h), is now properly named for each instance of the component.

Altium Designer 10 Update 8 (Platform Build 10.577.22514) – June 14, 2011

System Components: Altium Designer Base

2532	Cutouts no longer generated on mechanical and drill layers in PCB print based outputs. View BugCrunch report.
5044	In the PCB Release view, an error message is produced if the target output folders can not be deleted prior to output generation. View BugCrunch report.

System Components: PCB System

3940	Tracks/Arcs will no longer create incorrect Net Antenna violations when they are touching solid or hatched copper pour polygons.
4527	Dimensions referenced to an Embedded Board Array now show up properly when loading a design. View BugCrunch report.
4572	Copy Room Formats now correctly copies components when Selected Objects is checked and no longer generates no longer generates Channel Offset errors. View BugCrunch report.
4679	PCB Special strings used in bar-code text will now be correctly translated so the bar-code value will be that of the underlying text not the special string itself. View BugCrunch report.

5055	Pouring a copper polygon on a machine running a Korean OS will no longer freeze AD10.
5107	Dragging one or multiple selected tracks will again move the selection to the newly added tracks if any such tracks exist.

System Components: PCB Support

5015	CAMtastic® Preferences Default Layer Colours are no longer set indiscriminately to BLACK.
5042	CAMtastic® dialogues "Create NC Drawing", "Edit Array" & "Panelization" will now work correctly when Metric units are used.

Importers and Exporters: Importer - Allegro

3588	Allegro Importer - Component pads that have shapes and sizes that differ across top, middle, and bottom layers are now imported with their shapes and sizes intact.
4671	Allegro Importer - Objects with unrecognized GRAPHIC_DATA_NAME (such as DRC errors) no longer result in access violation.

Importers and Exporters: Importer – PADS

4869	PADS Importer - The description of PADS import files now properly includes PADS schematic libraries (*.P + *.C files).
4876	PADS Importer - ASCII files that contain simple line-feed record terminators (instead of standard carriage-return + line-feed) are now correctly processed.
4934	PADS Importer - Schematic part type definition alphanumeric pin-map information is now used properly to update the pins' pin designators, not their pin names.
5049	PADS Importer - Faulty Pin positions have been corrected for schematic designs with heterogeneous parts.
5051	PADS Importer - PCB library layer mapping dialog right-mouse popup now allows multi-selected PADS layers to be mapped to the full list of Altium Designer PCB Mechanical layers.

Output Generators: Output - STEP

4855	Fixed issue where PcbDoc's exported as STEP would load incorrectly into Catia. View BugCrunch report.

Output Generators: Printer - PCB

2532	Cutouts no longer generated on mechanical and drill layers in PCB print based outputs. View BugCrunch report.

Altium Designer 10 Update 9 (Platform Build 10.589.22577) – July 12, 2011

System Components: Altium Designer Base

3171	The files now open within the library project for svndblib. View BugCrunch report #112. View BugCrunch report #156.
5156	The issue was fixed where variants containing non-fitted components were incorrectly affecting the drill table hole counts in pcb prints and pdfs.

System Components: PCB System

2071	Small necks in a polygon pour that are less than the "Remove Necks" option are now properly removed.

3167	Fixed polygon pour thermal relief generation to only generate thermal reliefs if the thermal relief fully connects to the main polygon pour. View BugCrunch report.
4446	The interactive router loop removal now removes the correct track(s) in the case of co-located SMD pads. View BugCrunch report.
4447	The interactive router no longer performs the "Cleaning Net xxx" at the end of the route, which resulted in slowdowns for large nets.
4473	The interactive router Autocomplete function no longer deletes sections of adjacent tracks and vias.
4474	The interactive router loop removal is now removing the correct segments when routing from an antenna that has a junction (Y connection) further back in the route.
4544	An issue has been resolved where the conflict resolution mode was not remembered after subsequent drag operations. View BugCrunch report.
4783	Improvements to the interactive router loop removal routines for reported cases where loops had not successfully been removed.
4888	"Restore (n) Shelved Polygons" command will now ask the user if the un-shelved polygons need to be re-poured straight away or not. View BugCrunch report.
5088	The Multiroute and Diff pair tools no longer appear to freeze or hang when routing close to a very large keepout arc.

System Components: PCB Support

5125	CAMtastic® QuickLoad command will no longer stop loading when .APR_LIB files are found in the loading directory.

System Components: Schematic System

5169	It is now possible to choose an alternative footprint for a vault component.
5189	A crash no longer occurs when updating parts from a vault in certain conditions.

System Components: Soft Design Support

2905	Xilinx constraint file import has been improved. Drive strength and slew rate constraint from UCF files are properly imported now.

FPGA Components: FPGA Configurable - Wishbone Memory Controller

3508	SDRAM controller produces correct netlist for 32bit memory layout when memory size is set to 8MB.
4376	Missing Shared Memory Controller template for 2x16bit sram configuration is included in Altium Designer.

Output Generators: Printer – PCB

5156	The issue was fixed where variants containing non-fitted components were incorrectly affecting the drill table hole counts in pcb prints and pdfs.

Altium Designer 10 Update 10 (Platform Build 10.600.22648) – July 28, 2011

System Components: PCB System

4772	Angular dimensions will now be correctly saved always no matter how the inside/outside reference points are selected. View BugCrunch report.

System Components: PCB Support

5179	CAMtastic® Rotate/Mirror commands will no longer throw "Invalid parameter" exception when rotating/mirroring custom apertures if COMMA is the decimal separator.
5198	CAMtastic® "Build Drill Layer (PTH)" command will no longer create drill points that are invisible if the composite number of the copied flashes is greater then the new drill layer.
5199	CAMtastic® "Edit / Objects / Change/Modify" command will now work correctly if the user chooses to move the modified objects to a new layer.

System Components: Schematic System

4736	Implemented "Select touching area" and "Select touching line" for object selection in schematic sheets, libraries and OpenBus documents.View BugCrunch report.
5212	It is now possible to reset component designators when copying and pasting in schematic. To enable this behaviour, go to the preference Schematic >> Graphical Editing and check the 'Reset Parts Designator On Paste' checkbox. When components are pasted, their designators will be reset to '?'. View BugCrunch report.

Altium Designer 10 Update 11 (Platform Build 10.651.22821) – September 15, 2011

System Components: Altium Designer Base

5294	Display the license Subscription Status and date.

System Components: Altium Designer Installation System

5294	Display the license Subscription Status and date.

System Components: Altium Designer Localization

5041	Japanese localization of Altium Designer updated. View BugCrunch report #898.
5056	Simplified Chinese localization of Altium Designer updated.
5057	Korean localization of Altium Designer updated.
5365	Traditional Chinese localization of Altium Designer updated.
5376	French and German localization of Altium Designer updated.

System Components: PCB System

4846	When creating a PDF in the OutJob from a 3d Print job, the PCB editor no longer keeps the board flipped. View BugCrunch report #387.
5258	Streamline the operation of "Configure Physical Nets" batch dialogue so it allows multi-selection & update of multiple rows & also speed-up the display of the RMB pop-up for design with more than 500 nets.
5298	A crash that used to happen while resizing split planes by moving track vertices will no longer occur.

Importers and Exporters: Importer - Allegro

5268	Allegro Importer - A recent modification to correct import of differing Top-Mid-Bottom pad shapes impaired proper creation of some single-layer SMD pads. Single-layer SMD pads are now imported correctly.

Importers and Exporters: Importer - PADS

4862	PADS Importer - Pad and via test points are now detected and properly processed during import of PCB designs.
4926	PADS Importer - Zero sized pads are now discarded during import of pcb designs and libraries, with messages to the log file.
5052	PADS Importer - When importing PADS pcb designs and libraries, mapping every layer is no longer mandatory.
5188	PADS Importer - Differential pair rules are now more reliably imported from PADS pcb designs.

Output Generators: Output - AdvPcb3DPrint

4846	When creating a PDF in the OutJob from a 3d Print job, the PCB editor no longer keeps the board flipped. View BugCrunch report #387.

Output Generators: Output - Gerber

5118	An error when generating ODB++ from PCB designs that have components with invalid 3D Body Snap Point count has been fixed.
5283	An access violation that used to happen when generating ODB++ for PCB designs containing Embedded Board Arrays (EBA) that used mechanical layers > than Mechanical Layer 16 will no longer occur.
5302	ODB++ Output now correctly exports components that have the reference point different from any of the pads (e.g. component centre).

Output Generators: Output - ODB

5118	An error when generating ODB++ from PCB designs that have components with invalid 3D Body Snap Point count has been fixed.
5283	An access violation that used to happen when generating ODB++ for PCB designs containing Embedded Board Arrays (EBA) that used mechanical layers > than Mechanical Layer 16 will no longer occur.
5302	ODB++ Output now correctly exports components that have the reference point different from any of the pads (e.g. component centre).
5316	ODB++ output no longer generates incorrect image & eda package data for offset rounded pads. View BugCrunch report #734.

Altium Designer 10 Update 12 (Platform Build 10.700.22943) – October 10, 2011

System Components: Altium Designer Base

4530	No ERC Directives in schematic have been enhanced and can now suppress specific violations. Only the selected warning or error conditions are suppressed and any other warning or error will be detected and reported. View BugCrunch report #152.
4978	Added the options to include all notes, exclude collapsed notes, or exclude all notes from print and PDF outputs. View BugCrunch report #459.
4998	An issue whereby a Japanese text field was truncated in the Bill of Materials report has been resolved. View BugCrunch report #472.
5347	An issue with saving and loading localization preferences has been fixed. View BugCrunch report #822.

5406	The "Update from PCB library" command now shows differences between pad holes. View BugCrunch report #874.

System Components: Altium Designer Support

4961	An issue where by a Protel 99SE ddb file saved in a Non English version Windows XP would crash on load has been resolved.

System Components: PCB System

4856	The board insight display panel now redraws the preview panel to match the primitives as they are added to the panel on hover. View BugCrunch report #322.
5000	An issue has been resolved whereby PcbDoc files containing dimensions would crash when opened on Windows XP Japanese
5353	Fixed problem with very large polygon pour thermal spokes potentially causing clearance violations. View BugCrunch report #853.
5386	An issue has been resolved whereby PCB Binary 4.0 Files containing Coordinate Objects would crash on loading. The error was identified where an intermediate PCB Binary 4.0 file was generated during the process of importing a 99SE file. View BugCrunch report #859.
5406	The "Update from PCB library" command now shows differences between pad holes. View BugCrunch report #874.
5410	Net on shelved polygon is now correctly updated when updated from Schematic document. View BugCrunch report #612.
5411	PCB DRC now issues warning if document contains shelved polygons. View BugCrunch report #666.

System Components: PCB Support

5412	Following the use of the IPC® Compliant Footprint Wizard, some operations on the PCB library document caused unstable conditions unless the library was closed and re-opened. This has been resolved. View BugCrunch report #869.

System Components: Schematic System

4530	No ERC Directives in schematic have been enhanced and can now suppress specific violations. Only the selected warning or error conditions are suppressed and any other warning or error will be detected and reported. View BugCrunch report #152.
4978	Added the options to include all notes, exclude collapsed notes, or exclude all notes from print and PDF outputs. View BugCrunch report #459.
5275	Fixed an issue where zero-size ellipses and arcs were erroneously selected.

System Components: Soft Design System

5134	Published Core Projects now include all vhdl files for Altera target. View BugCrunch report #791.
5391	FPGA_DELAY_MAX, FPGA_DELAY_MAX_TO and FPGA_DELAY_FROM handling has been improved. Bus values are correctly passed to UCF file. View BugCrunch report #512. View BugCrunch report #567.

System Components: Soft Design Support

5134	Published Core Projects now include all vhdl files for Altera target. View BugCrunch report #791.
5264	Wishbone interconnect has been improved. Multicycle peripherals are handled correctly.

FPGA Components: Instrument - Digital IO

1668	DigitalIO ports are correctly named when more than 26 ports are added. Port names are valid hdl identifiers and are not causing build errors.

Importers and Exporters: Importer - CADSTAR

3650	The CADSTAR importer has been fixed so that it can now handle invalid characters in sheet filenames.

Importers and Exporters: Importer - PADS

4863	PADS plane and mixed signal/plane layer types are now detected more reliably and initialized in the layer map as internal plane layers, when appropriate.
5419	Removed indication from dialogs that all used PADS layers must be mapped, as this is no longer required.
5435	Part decals that include pieces of type 'TAG' are now properly read by the PADS Importer, and cease to ultimately cause access violations.
5443	Pcb design import now creates solid regions on plane layers to produce copper void areas where appropriate.

Output Generators: Output - ERC

4530	No ERC Directives in schematic have been enhanced and can now suppress specific violations. Only the selected warning or error conditions are suppressed and any other warning or error will be detected and reported. View BugCrunch report #152.

Output Generators: Output - NC-Drill

5404	A new option was added to NCDrill Settings dialogue that will allow the user to output the EIA Binary Drill file or not. The default for this option is to not generate this NCDrill output type. View BugCrunch report #706.

Output Generators: Output – STEP

5405	Fixed issue where PcbDoc with circular holes exported as STEP would load incorrectly into Catia. View BugCrunch report #328.

Output Generators: Printer - Schematic

4530	No ERC Directives in schematic have been enhanced and can now suppress specific violations. Only the selected warning or error conditions are suppressed and any other warning or error will be detected and reported. View BugCrunch report #152.

Altium Designer 10 Update 13 (Platform Build 10.747.23074) – November 10, 2011

System Components: Altium Designer Base

5489	Floating Net Label violations are no longer raised for inferred net labels.

System Components: Altium Designer Support

5531	Introduced a patching system to dramatically reduce the dowload size for updates. To use the patching with this update, please read instructions.

System Components: PCB System

5422	3D Body STEP models will no longer cause crashes because of multi-threading contentions while creating/deleting temporary STEP model files needed for mesh generation.
5488	All TrueType Text hidden in the PCB Graphical View will now be correctly output to Gerber & ODB++. This is the default behaviour when using Stroke Text.
5490	Mask Level control in PCB editor widened to prevent display value cut-offs when value was set to '100%'. View BugCrunch report #475.

System Components: PCB Support

5544	STEP Output will be correctly generated when ran after a Gerber, ODB++ or IPC CAMtastic® file load if the current OS locale is COMMA. View BugCrunch report #1004.

System Components: Schematic System

4958	Mirrored and rotated components in version 4 schematic files are now imported correctly.
5272	Schematic menu item Select > Touching Area renamed to Select > Touching Rectangle for consistency with PCB menu.
5315	Schematic text rendering has been improved to make text size resolution independent, and so that the print copy better matches what is seen the screen. View BugCrunch report #313.
5517	Holding the Ctrl key while manipulating non-electrical objects now temporarily sets the schematic snap grid to the finest setting. View BugCrunch report #984.
5518	The Find Similar Objects dialog now includes an option to update the Inspector to the same scope. View BugCrunch report #742.
5527	Fixed crash when importing Protel 99SE schematics

System Components: Soft Design Support

5588	Altera pin file importer has been improved. Reserved fpga pins are no longer imported into Altium Constraint file.
5589	Altera pin file importer has been improved. Device migration information is not translated as part of the process.

Hardware Support Packages: Device Support - Altera Stratix III

5581	Altera Stratix 3 support has been improved. EP3SL200F1517 package includes correct iostandard information for pins in banks 1B, 2B, 5B, 6B.
5642	Altera Stratix3 device support has been improved. Differential pair N32/N33 polarity for 1157 package has been corrected.

Importers and Exporters: Exporter – IDF

1860	The IDF exporter now supports board cutouts.
1861	An issue has been corrected in the IDF exporter whereby the thickness calculated for the generated IDF board file differed from the source PcbDoc.
5546	The IDF exporter now allows the file extensions of the generated board and library files to be changed in the settings.
5547	The IDF exporter now includes an option to exclude small holes from the generated board file.

Importers and Exporters: Importer - IDF

Required due to dependencies in updates made to Exporter - IDF module.

Output Generators: Output – ODB

5488	All TrueType Text hidden in the PCB Graphical View will now be correctly output to Gerber & ODB++. This is the default behaviour when using Stroke Text.

Altium Designer 10 Update 14 (Platform Build 10.771.23139) – November 23, 2011

System Components: Altium Designer Base

5177	Improved performance of "Find Partial Matches" stage of document comparator
5530	Detection of duplicate designator and sub-part violations during scrap compile has been fixed. View BugCrunch report #606.
5593	The ECO dialog no longer warns about errors if they have all been suppressed
5751	Fixed crash that occurred when right-clicking an empty messages panel. View BugCrunch report #1174.

System Components: PCB System

4510	PCB Editor's ECO process now performs net assignment changes for all same-name component pads. View BugCrunch report #146.
4681	The interactive routing tools now honor the "Routing Layers" rule, and the rule is DRC. View BugCrunch report #251.

System Components: Schematic System

5533	A bug that allowed non-zero rotation of library components has been fixed. View BugCrunch report #223.
5694	An access violation due to negative font sizes in imported schematics has been fixed.
5730	Text rendering in exported DXF and DWG files has been fixed.

System Components: Soft Design Support

5254	A positional association in a port map of a component that is not declared may crash the vhdl parser. This is fixed. View BugCrunch report #528.

Importers and Exporters: Exporter - AutoCAD DWG

5535	AutoCAD DXF/DWG exports can now be included in output job files. View BugCrunch report #672.
5730	Text rendering in exported DXF and DWG files has been fixed. View BugCrunch report #1142.

Importers and Exporters: Exporter – DXF

5535	AutoCAD DXF/DWG exports can now be included in output job files. View BugCrunch report #672.

Importers and Exporters: Exporter – Hyperlynx

2634	The PCB Editor Save As... Export HyperLynx format utility now exports solid regions, polygon pours, and planes.
5514	Tiny arcs whose start and end points evaluate as coincident are now omitted, so that they are not mistaken for full circles.

5515	Layer and net names that contain special characters are now detected more consistently, and double-quotes are used as required.
5520	Rounded rectangle pad shapes are now correctly represented in the exported .hyp file.

Importers and Exporters: Importer – Allegro

5374	Bottom layer SMD pads are now imported correctly as simple mode padstacks.
5596	Polygon and filled shape objects residing on internal plane layers now import as split planes, and framing geometry is added to make them persistent.

Importers and Exporters: Importer – PADS

5525	Application of pad offset has been corrected and improved.
5526	Processing of DIF_PAIR design rules of v9.3 have been corrected.
5548	Processing of DIF_PAIR definition now correctly creates routing width rules.

Output Generators: Output - NC-Drill

5683	Corrected problem where rotated holes in embedded board arrays would produce incorrect NC drill output. View BugCrunch report #1075.

Output Generators: Output - Gerber

5491	The outermost pads of a blind/buried via are now generated, regardless of the option "Include unconnected mid-layer pads". View BugCrunch report #650.

Output Generators: Output – STEP

5492	The STEP Outjob now supports variants. View BugCrunch report #192.

Altium Designer 10 Update 15 (Platform Build 10.818.23272) – December 19, 2011

Key highlights

Custom pad shapes

As a result of the very first BugCrunch report that was voted in, this latest update adds the ability to add solder and paste mask expansion rules to regions, fills, and tracks. So now you can attach virtually any copper geometry to a pad and give it ‘pad-like’ solder and/or paste mask expansions. More information. View BugCrunch report #67.

Loop removal improvements

The Advanced Interactive Router's loop remove algorithm has been improved which will fix a variety of known issues as well as deliver better overall results. View BugCrunch report #132. View BugCrunch report #425. View BugCrunch report #596.

Print from PCB Library

This was the second issue to get voted through in BugCrunch and also very popular. So we've implemented the request and footprints can now be printed directly from a PCB library. View BugCrunch report #109.

Designators movable by multiple selections in PCB

Again, a popular item in BugCrunch. So, moving multiple component designators is now supported in PCB using the Move>>Selection command. View BugCrunch report #1089.

Additional FPGA Vendor Constraints and Device Support

This update includes added support for Altera's Max V and Stratix IV CPLD/FPGA devices. In addition to this, Altium Designer's constraint files have been significantly revamped to include support for a large array of extra Vendor constraints. This will let you continue creating vendor-neutral FPGA designs using the latest IO standards from within Altium's Unified Design Environment.

Proxy scripts supported

If you have had problems previously with installing and updating AD10 because of access through proxy servers, we've implemented a couple of fixes that should now resolve those issues. Instructions for deploying improved proxy support. View BugCrunch report #103.

The new Altium Installer and Download Manager require Internet Explorer 7 or later to be installed on your PC. If you have earlier versions, or do not have it installed, you will not be able to install successfully, or to update after this release.

System Components: Altium Designer Base

5709	FPGA Signal Manager has been improved. IO Standard constraints are correctly translated to Altium Constraint file.
5794	The issue causing blank pdf pages in schematic outputs under certain circumstances has been fixed.

System Components: Altium Designer Installation System

4437	AltiumInstaller and AltiumDownloadManager are updated with improved Proxy support. Proxy server settings must be configured in Internet Explorer's Internet Options > Connections > LAN Settings. Manual proxy sign-ins are not supported. Instructions for deploying improved proxy support.
4438	AltiumInstaller and AltiumDownloadManager have improved support for automatic configuration script files setup in Internet Explorer's Internet Options. Instructions for deploying improved proxy support. View BugCrunch report #103.

System Components: Data Management

5781	Changed warning displayed during connection to Vault dialog to be based on license subscription instead of AltiumLive plan.

System Components: PCB System

3565	Fixed PCB problem where Y coordinate of custom board origin and dimensions was reset if Hungarian Locale was used. View BugCrunch report #673.
3567	Resolved Paste Special issue of multiple nets on different layer
4452	Footprints can now be printed from a PCB library. View BugCrunch report #109.
4794	Fixed the Advanced Interactive Router to properly handle room specific clearance rules when in Walkaround Obstacles mode.
5329	TANGO ASCII file format importer will now work as expected.
5401	Added loop remove shortcut (Shift-D) to the Advanced Interactive Routers. View BugCrunch report #596.
5539	Non pad primitives have been given the applity to generate mask layer expansions when they are on the top or bottom layers. This will simplify the creation of complex pad shapes. More information. View BugCrunch report #67.
5543	Fixed a variety of problems with Advanced Interactive Router's loop remove algorithm. View BugCrunch report #132. View BugCrunch report #425.
5722	Fixed PCB crash when deleting component with.Designator special string which was in violation with another silkscreen object.

5752	Moving multiple component designators is now supported in PCB using the Move>>Selection command. View BugCrunch report #1089.

System Components: Schematic System

5679	Fixed slowness experience by some users on copy. View BugCrunch report #1182.
5793	Tabbed text in text frames is now rendered correctly with Render text with gdi+ option on.

System Components: Soft Design Support

2598	A parameterized blackbox module is instantiated correctly also if the blackbox is instantiated multiple times where each instantiation assigns a different value, or the default value. I.e. the different parameter values are stored in the EDIF file.
4426	Altium Core Generator has been improved. Internal block memory supports hex file initialization for memories larger than 64K.
4622	Unisim library support updated, now compatible with Xilinx V13.3.
4904	An incorrect VHDL condition with OTHERS could cause a failed assertion and then an access violation
5098	Altera Stratix 4 device support has been added to Altium Designer.
5606	Altera Max 5 device support has been added to Altium Designer.
5666	SSTL15I IO standard is translated to Altera "SSTL-15 CLASS I" constraint.
5667	SSTL15II IO standard is translated to Altera "SSTL-15 CLASS II" constraint.
5668	DSSTL15I IO standard is translated to Altera "DIFFERENTIAL 1.5-V SSTL CLASS I" constraint.
5669	DSSTL15II IO standard is translated to Altera "DIFFERENTIAL 1.5-V SSTL CLASS II" constraint.
5671	Altera Stratix 3 IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5672	Altera Stratix 2GX IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5675	Altera Stratix 4 IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5676	Altera Max 5 IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5710	Add/Modify Port Constraint dialog has been updated. IO Standards use descriptive names for display in combo box.
5711	Altera pin file importer has been improved. 3.3V LVCMOS and LVTTL iostandards are imported correctly.

System Components: Soft Design Synthesis Libraries

4622	Unisim library support updated, now compatible with Xilinx V13.3.

System Components: Soft Design System

2598	A parameterized blackbox module is instantiated correctly also if the blackbox is instantiated multiple times where each instantiation assigns a different value, or the default value. I.e. the different parameter values are stored in the EDIF file.
4622	Unisim library support updated, now compatible with Xilinx V13.3.
4904	An incorrect VHDL condition with OTHERS could cause a failed assertion and then an access violation
5098	Altera Stratix 4 device support has been added to Altium Designer.
5425	Core Project outputs handling has been improved. Vhdl macrocell outputs from Altium Synthesizer are copied across to linked fpga project. View BugCrunch report #791.

5436	FPGA_CLOCK constraint handling has been improved when XST synthesizer is used.
5437	FPGA_CLOCK_PIN constraint handling has been improved when XST synthesizer is used.
5438	FPGA_CLOCK constraint handling has been improved when XST synthesizer is used. When set to FALSE it will prevent XST from using clock buffer on object it has been applied to.
5439	FPGA_CLOCK_PIN constraint handling has been improved. When used with XST synthesizer and set to False it will prevent XST from inserting ibufg primitive on port it has been applied to.
5440	FPGA_CLOCK constraint handling has been improved. When used with Quartus synthesizer and set to True it will enforce Quartus to use global buffer.
5441	FPGA_CLOCK constraint handling has been improved. When set to False and used with Quartus synthesizer it will prevent usage of global buffer.
5447	FPGA_CLOCK constraint handling has been improved. When used with Synplify will enforce global clock buffer insertion.
5448	FPGA_CLOCK_PIN constraint handling has been improved. When used with Synplify synthesizer will enforce clock buffer usage.
5449	FPGA_CLOCK constraint handling has been improved. When set to False and used with Synplify synthesizer it will prevent global buffer insertion.
5450	FPGA_CLOCK_PIN constraint handling has been improved. When set to False and used with Synplify it will prevent synthesizer from using global clock buffer.
5471	FPGA_CLOCK_FREQUENCY constraint handling has been improved. When used with Synplify synthesizer it will request timing based synthesis. Applies to standalone, Actel and Lattice version.
5473	Xilinx Bit Generation build step has been improved. Bitgen DRC is run against design autogenerated pcf constraint.
5496	Linking Core project to FPGA project no longer requires device specific configuration for the core project to build them without publishing.
5505	FPGA_CLOCK_FREQUENCY constraint is correctly handled when used with Synplify targeting Actel devices.
5507	FPGA_CLOCK_FREQUENCY constraint handling for Actel devices has been improved. Net objects are handled correctly.
5606	Altera Max 5 device support has been added to Altium Designer.
5608	When unsupported IO standard is applied in Altium constraint file to Altera target Altium Designer will issue warning.

FPGA Components: FPGA Configurable - Generic Logic

5098	Altera Stratix 4 device support has been added to Altium Designer.
5606	Altera Max 5 device support has been added to Altium Designer.

FPGA Components: FPGA Configurable - Wishbone Memory Controller

5498	Shared USB controller template has been improved. Wishbone acknowledge line is asserted for single clock cycle only.

FPGA Design Tools: Ancillary VHDL Synthesis Libraries

5610	DHSTL18I IO Standard is mapped to Altera "DIFFERENTIAL 1.8-V HSTL CLASS I" constraint.
5611	DHSTL18II IO standard is mapped to Altera "DIFFERENTIAL 1.8V HSTL CLASS II" constraint.
5612	DHSTLI IO Standard is translated to Altera "DIFFERENTIAL 1.5-V HSTL CLASS I" constraint.
5613	DHSTLII IO standard is translated to Altera "DIFFERENTIAL 1.5-V HSTL CLASS II" constraint.
5614	LVCMOS12 IO standard is translated to Altera "1.2 V" constraint.
5615	BLVDS25 IO standard is translated to Altera "BUS LVDS" constraint.
5616	LVDS_E_3R IO standard is translated to Altera "LVDS_E_3R" constraint.
5617	LVDS_E_1R IO standard is translated to Altera "LVDS_E_1R" constraint.

5618	MINILVDS25_E_1R IO standard is translated to Altera "MINI-LVDS_E_1R" constraint.
5619	MINILVDS25_E_3R IO standard translates to Altera "MINI-LVDS_E_3R" constraint.
5620	RSDS25_E_1R IO standard translates to Altera "RSDS_E_1R" constraint.
5621	RSDS25_E_3R IO standard translates to Altera "RSDS_E_3R" constraint.
5622	LVTTL12 IO standard translates to Altera "1.2 V" constraint.
5623	RSDS33 IO standard translates to Altera "RSDS" constraint.
5624	LVCMOS30 IO standard translates to Altera "3.0-V LVCMOS" constraint.
5625	LVTTL30 IO standard translates to Altera "3.0-V LVTTL" constraint.
5626	PCML12 IO standard translates to Altera "1.2-V PCML" constraint.
5627	PCML14 IO standard translates to Altera "1.4-V PCML" constraint.
5628	PCML25 IO standard translates to Altera "2.5-V PCML" constraint.
5629	HCSL IO Standard translates to Altera "HCSL" constraint.
5630	PCI33_30 IO standard is translated to Altera "3.0-V PCI" constraint.
5631	PCIX_30 IO standard is translated to Altera "3.0-V PCI-X" constraint.
5632	PPDS25 IO standard is translated to Altera "PPDS" constraint.
5633	PPDS25_E_3R IO standard is translated to Altera "PPDS_E_3R" constraint.
5634	BLVDS33 IO standard is translated to Altera "BUS LVDS" constraint.
5635	Altera ArriaGX IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5644	Altera Cyclone IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5646	Altera Cyclone2 IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5648	DHSTL12I IO standard is translated to Altera "DIFFERENTIAL 1.2-V HSTL CLASS I" constraint.
5649	DHSTL12II IO standard is translated to Altera "DIFFERENTIAL 1.2-V HSTL CLASS II" constraint.
5650	HSTLI_12 IO standard is translated to Altera "1.2-V HSTL CLASS I" constraint.
5651	HSTLII_12 IO standard is translated to Altera "1.2-V HSTL CLASS II" constraint.
5652	Altera Cyclone3 IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5656	Altera Cyclone4E IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5657	Altera Cyclone 4GX IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5659	Altera Stratix IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5661	Altera Stratix 2 IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5665	Altera Stratix GX IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5666	SSTL15I IO standard is translated to Altera "SSTL-15 CLASS I" constraint.
5667	SSTL15II IO standard is translated to Altera "SSTL-15 CLASS II" constraint.
5668	DSSTL15I IO standard is translated to Altera "DIFFERENTIAL 1.5-V SSTL CLASS I" constraint.
5669	DSSTL15II IO standard is translated to Altera "DIFFERENTIAL 1.5-V SSTL CLASS II" constraint.

5671	Altera Stratix 3 IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5672	Altera Stratix 2GX IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5675	Altera Stratix 4 IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5676	Altera Max 5 IO standard export/import has been improved. All io standards supported by this device can be exported from Altium constraint file and imported from Altera pad file.
5711	Altera pin file importer has been improved. 3.3V LVCMOS and LVTTL iostandards are imported correctly.

Hardware Support Packages: Device Support - Altera Max V (New Module)

5606	Altera Max V device support has been added to Altium Designer. Download Altera Max V Integrated Libraries

Hardware Support Packages: Device Support - Altera Stratix IV (New Module)

5098	Altera Stratix 4 device support has been added to Altium Designer. Download Altera Stratix IV Integrated Libraries

Importers and Exporters: Importer - Tango-PCB ASCII file

5329	TANGO ASCII file format importer will now work as expected.

Output Generators: Output - ERC

5724	ERC Report output job option default for Report Suppressed Errors changed to False to be consistent with default project option

Output Generators: Output - Gerber

5539	Non pad primitives have been given the applity to generate mask layer expansions when they are on the top or bottom layers. This will simplify the creation of complex pad shapes. More information. View BugCrunch report #67.
5754	Gerber Output for flipped embedded board arrays that have components with rotated offset pads has been corrected.
5805	"Drill symbol limit exceeded" modal dialog is now supressed and warning logged to messages panel instead. View BugCrunch report #652.

Output Generators: Output – ODB

5539	Non pad primitives have been given the applity to generate mask layer expansions when they are on the top or bottom layers. This will simplify the creation of complex pad shapes. More information. View BugCrunch report #67.

Output Generators: Printer – PCB

4452	Footprints can now be printed from a PCB library. View BugCrunch report #109.
5539	Non pad primitives have been given the applity to generate mask layer expansions when they are on the top or bottom layers. This will simplify the creation of complex pad shapes. More information. View BugCrunch report #67.
5805	"Drill symbol limit exceeded" modal dialog is now supressed and warning logged to messages panel instead. View BugCrunch report #652.

Development updating various modules

The development made for the following tickets required changes to our Run Time Libraries, and as a result require majority of the modules to be updated.

4303	Embedded Threads debugging panel is working again (was always empty in R10).
5098	Altera Stratix 4 device support has been added to Altium Designer.
5309	An Access Violation with message "List index out of bounds (-1)" will no longer occur when using any of the grid (tree list view) controls when the memory used by AD is close or over ***2GB***.
5586	Access violation on close when a LibPkg is added as a pcb project source document has been fixed
5606	Altera Max 5 device support has been added to Altium Designer.
5689	Altera pin file importer has been improved. Pin file parser correctly imports pin information from Altera pin description tables.
5781	Changed warning displayed during connection to Vault dialog to be based on license subscription instead of AltiumLive plan
5785	The preferences dialog has been improved so that all controls are accessible on lower resolution wide screens, which typically have lower vertical resolutions. View BugCrunch report #482.

Altium Designer Update 16 (Platform Build 10.890.23450) – February 6, 2012

Key highlights

Improvement to impedance and width calculations

This release delivers enhanced control for High Speed signal routing in Altium Designer through improvements in the application of trace routing rule calculations. These can be found in the Impedance Formula Editor in the Layer Stack Manager, which now offers more accurate default formulas for impedance and width calculations. View BugCrunch report #201.
Specifically, to provide better control for material layers, new variable keywords have been added to the equation Helper including:
ErAbove; *ErBelow* – define material above or below the trace.
DielectricHeightAbove; DielectricHeightBelow – define dielectric thickness above or below the trace.

Export Free Pad Holes

Altium Designer's support for STEP files allows detailed and accurate modeling data to be interchanged with mechanical CAD and 3D modeling programs. When defining an OutJob for exporting STEP files, a new option has been added to "Export Free Pad Holes" in addition to the existing options to export electrical and mechanical component holes. Designers using Free Pad Holes for board mounting or other purposes can now easily pass this information into the MCAD domain via an exported STEP file.

System Components: Altium Designer Base

5171	Fixed an issue where locked physical designators were not applied correctly.
5831	Fixed crash on document close.
5856	Fixed an issue where preferences for New Document Defaults were not always loaded correctly. View BugCrunch report #1191
5905	Fixed a regression issue where multi-channel annotations were not displayed correctly in schematics.

System Components: Altium Designer Installation System

5848	Fixed an issue that was causing intermittent application freezing / lockups.

System Components: PCB System

4604	Fixed an issue where scripts using the Round function stopped working.
4638	More accurate default formulas provided for characteristic impedance and width calculations. Added additional keywords ErAbove, ErBelow, DielectricHeightAbove, DielectricHeightBelow. View BugCrunch report #201
5025	An issue causing Ansoft SIWave to report DC Shorted net errors in exported file on some plane layer connections has been fixed.
5552	Fixed an issue where scripts using the Round function stopped working.
5824	Fixed loop remove crash with hatched polygon pours.
5863	An issue whereby the solder mask expansion and paste mask expansion properties for regions were incorrectly loaded from PcbDoc files has been resolved.
5878	Fixed crash on AD shutdown after editing Dimension defaults in PCB.

System Components: Schematic System

5762	The size of the negation bar drawn over a space character has been fixed.
5829	Fixed an issue where variants were not correctly applied when components had parts on multiple sheets. View BugCrunch report #267
5905	Fixed a regression issue where multi-channel annotations were not displayed correctly in schematics.

FPGA Design Tools: Aldec Simulator

5847	Aldec OEM Simulator license file has been updated.

Importers and Exporters: Exporter - Ansoft

5025	An issue causing Ansoft SIWave to report DC Shorted net errors in exported file on some plane layer connections has been fixed.
5026	No Net primitives are now correctly handled upon import to Ansoft - SIWave, and no longer cause disjointed net errors.

Output Generators: Output - Gerber

5826	An Access Violation that used to happen when generating Gerber Output if "Use Software Arcs" option was ON has now been fixed.

Output Generators: Output – STEP

4767	An "Export Free Pad Holes" option has been added to the Export STEP outjob.

Output Generators: Printer – Schematic

5905	Fixed a regression issue where multi-channel annotations were not displayed correctly in schematics.

Altium Designer Update 17 (Platform Build 10.972.23595) – March 21, 2012

Key highlights

Via Stitching

Of particular importance for RF and High Speed designs, the brand new Via Stitching feature applies a definable pattern of vias between layers where the copper areas overlap and share the same net. It helps maintain low impedance connections and short return loops through the board structure for developing high-performance, electromagnetically 'quiet' PCBs.

Via Stitching runs as a post-process using an algorithm that identifies all Fills, Polygons and Power Planes attached to a specified net, then populates free areas of copper with stitching vias to connect the layers using the specified via and stitching pattern. See the Wiki page for more information or watch the video on this new feature.

Schematic text overlay rendering

Text container frames placed on the Schematic have been improved to display and print as the uppermost level, regardless of any electrical drawing primitives that the frame overlays. View BugCrunch report #1172.

Improvements to Ansoft Exporter

In update 16 we released improvements to this exporter to make it easier to import and simulate in Ansoft products. With this latest update, we've continued development and reduced the number of errors generated once imported into Ansoft (object centreline connection issues, and reducing differences between metric and imperial exports). Also, a larger array of component values is now imported, making it easier to set up the board for simulation.

Improvements to software update patching system

The Altium Designer software patching system has been further enhanced to make the software update process less disruptive. Amongst a range of improvements, the patch preparation process has been configured to run during the update download at a low background priority, allowing Altium Designer to continue being used with minimal interruption. The update process now also provides the option to select whether you want to update using patches or a full download. This improvement will help those users who experience a lengthy update process due to anti-virus programs, where using the full download becomes a much faster process. Note: These improvements will only be visible with the next update to Altium Designer.

System Components: Altium Designer Base

5529	Fixed bugs in loading and saving preferences. View BugCrunch report #619. View BugCrunch report #1070.
5561	Updated logic for detecting violations for floating net labels, power objects and wires. View BugCrunch report #1488.

System Components: Altium Designer Installation System

5830	The patching system has been moved into the Altium Downloader to run in the background. Note: This improvement will only be visible with the next update to Altium Designer.
6012	Included an option when installing an update to use patches or a full download. Note: This option will only be visible for future updates.

System Components: PCB System

5528	Via stitching has been added. Refer to Altium Wiki for more information.

System Components: Schematic System

5686	Fixed slow drawing of schematics containing blankets with dashed linestyle.
5886	Junctions no longer display on top of text frames and notes. View BugCrunch report #1172.

5938	Fixed crash when compiling OpenBus documents.

Importers and Exporters: Exporter – Ansoft

5023	The Ansoft exporter has been improved to reduce differences in errors and warnings between metric and imperial exported files.
5024	The Ansoft exporter has been improved to reduce the number of warnings given when trace enpoints and pad centres are misaligned.
5027	The Ansoft exporter now includes RLC component values in a format that imports into SIwave.

Importers and Exporters: Importer - PADS

5928	Importing from Pads Logic libraries now imports arcs correctly.

Output Generators: Output – Gerber

5911	Offset pads are now rendered correctly when mirror is used in PCB Print / Gerber outputs generation. View BugCrunch report #1420.

Output Generators: Printer – PCB

5911	Offset pads are now rendered correctly when mirror is used in PCB Print / Gerber outputs generation. View BugCrunch report #1420.

Altium Designer Update 18 (Platform Build 10.1051.23878) – April 27, 2012

Key highlights

STEP model preview
A visual preview is now available when selecting a 3D STEP model in the PCB or library editors dialog box, which helps browsing through options when embedding a 3D body. View BugCrunch report #185.

New track selection mode
A new Select Track command has been added that provides the option of selecting connected track segments on the current layer – in effect, to select connected copper until the layers change or a component pad is encountered. In addition, the Select Physical Connection option has been changed so that tracks covered by a component pad are included in the selection. View BugCrunch report #1110.

Show contents while moving large selections
Pasting and moving of large schematic selections has been improved so that once rendered, the contents remains visible while placement is made. View BugCrunch report #685.

Line style editing in Inspector Panel
The style of Lines (as opposed to wires) in a Schematic document can now be defined and edited in the Inspector Panel. View BugCrunch report #1044.

Improved Update from Libraries behavior
The 'Update from Libraries' command in the PCB editor now takes into account non-physical differences between footprints. Non-physical differences – such as pin numbers, 3D body colours, hole diameters, etc – are now also detected when a footprint (or a collection of footprints) is updated from a library. View BugCrunch report #311. View BugCrunch report #1390.

Numerous FPGA/Embedded enhancements

A significant number of enhancements were made to FPGA/Embedded Design in Altium Designer, including support for the ST Microelectronics M25P (SPI) family of serial flash devices and improvements to Software Platform.

Improved junction handling and rendering

Several improvements have been made to the way schematic junctions are displayed, generated and printed. The behavior of auto-junctions has been improved for several moving or replication operations where they are regenerated on the fly. Also, auto-junctions now render in solid form on mono-colour printouts. View BugCrunch report #693. View BugCrunch report #1111.

Revised net violation handling with repeated sheets

Using repeated or multiple schematic sheet entries, as is the case with multi-channel and hierarchical designs, no longer causes violation warnings triggered by net signals effectively having different names. View BugCrunch report #1054.

System Components: Altium Designer Base

4801	Embedded Project options dialog now also opens when Embedded Design Tools for the selected processor have not been installed.
4990	Repeatedly compiling an unmodified error-free FPGA project should no longer produce errors.
5129	The PCB Editor "Update From Libraries" command now takes into account non-physical differences between footprints. Examples of the non-physical differences now reported are Pin Numbers, 3D body colours. View BugCrunch report #311. View BugCrunch report #1390.
5375	An Access Violation that occurred on machines with limited video memory when using the PCB editor has been resolved.
5934	Output jobs no longer modify the absolute path used for backwards compatibility if saved without modifying the relative path. View BugCrunch report #1198.
5940	Repeated sheet entries no longer cause "Net with multiple names" violations. View BugCrunch report #1054.
5989	The project output path and log folder path will now update with the project name if set to their default values. View BugCrunch report #1379.

System Components: Altium Designer Installation System

5979	Uninstaller GUI has been improved to enable easier management of Altium Designer installations.
6068	Changes to remove the Release 10 branding.

System Components: Altium Designer Localization

5755	Japanese localization of Altium Designer updated. View BugCrunch report #1287. View BugCrunch report #1599.
5757	Traditional Chinese localization of Altium Designer updated.
5844	Korean localization of Altium Designer updated.
5845	Simplified Chinese localization of Altium Designer updated.

System Components: Altium Designer Resources

6068	Changes to remove the Release 10 branding.

System Components: PCB Support

6038	CAMtastic's Re-load Rules from PCB command will now work as expected. View BugCrunch report #452.

System Components: PCB System

4404	Improved performance when dragging via in push obstacle mode. View BugCrunch report #271.

4593	Implemented STEP model preview in model selection dialog. View BugCrunch report #185.
5129	The PCB Editor "Update From Libraries" command now takes into account non-physical differences between footprints. Examples of the non-physical differences now reported are Pin Numbers, 3D body colours. View BugCrunch report #311.View BugCrunch report #1390.
5375	An Access Violation that occurred on machines with limited video memory when using the PCB editor has been resolved.
5853	Polygon properties dialog will now correctly handle shelved polygons when invoked from polygon manager.
5942	Fixed freeze/hang with Interactive Differential Pair Router. View BugCrunch report #1084. View BugCrunch #1516.
5991	Fixed crash in Interactive Router caused when routing from a no-net pad. View BugCrunch report #1084.
6046	Added command to select connected copper on layer. View BugCrunch report #1110.
6047	Changed Board Information dialog to report number of violations on the board instead of number of primitives with violations which was confusing. View BugCrunch report #1533.
6048	Fixed problem where grid type was not saved correctly in PCB Library if dot drawing option was used. View BugCrunch report #485.

System Components: Schematic System

4697	Fixed an issue where 4-way junctions were optimized out during Ctrl-drag.
5534	Pasting and moving of large selections has been improved so that once drawn the contents remains visible while placement is made. View BugCrunch report #685.
5537	Fixed an issue where 4-way junctions were destroyed when the junction was moved or dragged to a new location. View BugCrunch report #693.
5976	Fixed an issue where 4-way junctions were lost when copy-pasting or duplicating part of a schematic. View BugCrunch report #1111.
6033	Fixed display and editing in schematic inspector for Line Style property. View BugCrunch report #1044.
6052	Fixed an issue where auto-junctions were not filled in on mono-color prints.

System Components: Soft Design Support

4990	Repeatedly compiling an unmodified error-free FPGA project should no longer produce errors.

System Components: Soft Design System

4801	Embedded Project options dialog now also opens when Embedded Design Tools for the selected processor have not been installed.
5297	Support for all M25P serial flash devices added.

Embedded Design Tools: Software Platform

4716	Software Platform Filesystem Mounting service plugin now has F1 help info.
4763	Multithreading Support Knowledge Center now has entries for all supported functions.
4782	Kernel function sched_yield() now returns 0 instead of -1 if there are no other equal priority threads to yield to.
5067	NiosII interrupt handler can now be located in external memory.
5081	Software platform builder no longer generates incorrect call to usb_open() routine.
5170	The pthread_setschedprio() routine from pthread.h has been implemented.
5312	POSIX Message Queue support no longer overwrites data when all slots in the queue are in use.
5702	A timeout on pthread_mutex_timedlock sets thread that timed out as current owner of the thread.
5887	POSIX write () function no longer fails on some very specific data size values (such as 32*1024 or 32*1024-1).

5896	Software Platform FAT filesystem implementation now supports statvfs() and fstatvfs() interfaces.
5917	When a FAT filesystem is mounted with SYNC flag, updates made through rename(), remove() or rmdir() are now directly written to the media.
5937	Parent (..) of directories created in the FAT filesystem root directory now point to cluster 0.

Importers and Exporters: Exporter - PCAD ASCII

6061	An access violation when loading and saving schematic libraries and schematics (projects) as P-CAD V16 ASCII has been fixed. View BugCrunch report #1262.

Importers and Exporters: Importer - Accel

6061	An access violation when loading and saving schematic libraries and schematics (projects) as P-CAD V16 ASCII has been fixed. View BugCrunch report #1262.

Output Generators: Output - AssyTestpoint

6049	Fixed problem with testpoint reports where bottom side test points were not reported properly - missing "099" code. View BugCrunch report #1370.

Output Generators: Output – Testpoint

6049	Fixed problem with testpoint reports where bottom side test points were not reported properly - missing "099" code. View BugCrunch report #1370.

Output Generators: Printer – PCB

6039	The variant "Not Fitted" crosses will no longer be missing on Assembly Drawing for Embedded Board Arrays. View BugCrunch report #270.

Development updating various modules

The development made for the following tickets required changes to our Run Time Libraries, and as a result require majority of the modules to be updated.

4200	Fixed painting of JTAG Viewer Panel.
4593	Implemented STEP model preview in model selection dialog. View BugCrunch report #185.
4700	Message text was sometimes stripped in messages panel if the length of the the output line generated by the tool exceeded a specific value.
4801	Embedded Project options dialog now also opens when Embedded Design Tools for the selected processor have not been installed.
5082	Embedded serial flash available in download dialog when using multiple SPI controllers.
5238	Select Symbol dialog in Embedded Code editor now also shows source file name.
5297	Support for all M25P serial flash devices added.
5375	An Access Violation that occurred on machines with limited video memory when using the PCB editor has been resolved.
5853	Polygon properties dialog will now correctly handle shelved polygons when invoked from polygon manager.
6061	An access violation when loading and saving schematic libraries and schematics (projects) as P-CAD V16 ASCII has been fixed. View BugCrunch report #1262.

Altium Designer Update 19 (Platform Build 10.1089.24016) – May 23, 2012

Key highlights

SubVersion 1.7 Support
Support for the latest version of Subversion has been added. This also includes support for the new working folder format, as well as updating the built-in Subversion Client to version 1.7.4. View BugCrunch report #838.

Improved proxy support
Users connecting to the Internet via a Proxy Server will now be able to get full access to all content stored in all of our Vaults & also any Vault they set-up & is cloud based. This will include downloading, uploading items and getting previews.

Added support for script parameters
It is now possible to add parameters to Projects and Project Variants through scripts. View BugCrunch report #1085.

Air gap attribute added
Added air gap attribute to Polygon Connect Style rule for finer gap control during polygon pouring process. Read Wiki information. View BugCrunch report #694.

Continued improvement to importers and exporters
This update includes additional improvements to the Hyperlynx exporter and the P-CAD importer. View BugCrunch report #799.

System Components: Altium Designer Base

6087	Multiple instances of sheet symbols no longer cause "Net with multiple names" violations.
6124	Fixed issue causing read only PDF files to be shown and opened as text documents. View BugCrunch report #1039.
6127	It is now possible to add parameters to Projects and Project Variants through scripts. View BugCrunch report #1085.
6136	A crash occurring when the Brady IP300 printer driver is installed has been fixed.
6142	Prevented "Add Project folder to Version Control" command from being run on documents in the free documents project as this project does not have a valid project folder. View BugCrunch report #1477.

System Components: Altium Designer Localization

6137	Updated Japanese localization of Altium Designer.
6143	Updated Traditional Chinese localization of Altium Designer.

System Components: Altium Designer Support

5678	Support for Subversion 1.7 added, including support for the new working folder format as well as updating the built-in Subversion Client to version 1.7.4. View BugCrunch report #838.

System Components: Data Management

4488	Users connecting to the Internet via a Proxy Server will now be able to get full access to all content stored in all of our Vaults & also any Vault they set-up & is cloud based. This will include downloading, uploading items, getting previews etc.

System Components: PCB Support

6117	CAMtastic no longer throws an Access Violation Exception if regional decimal separator is set to comma & the user tries to change the current grid using the G key to a new value from the list e.g. 0.500 mm. View BugCrunch report #1098.

System Components: PCB System

2333	The interactive routers now use the tenting property of the default via from Preferences. View BugCrunch report #1447.
4586	Report Measure Primitives now correctly ignores shelved polygons.
6093	Solder mask positive view of vias now draws correctly. View BugCrunch report #1308.
6120	Fixed problem where hatched polygons were missing some primitives. View BugCrunch report #695.
6129	Added air gap attribute to Polygon Connect Style rule for finer gap control during polygon pouring process. Read Wiki information. View BugCrunch report #694.
6163	Routed nets are now properly copied across destination rooms using the Design>>Rooms>>Copy Room Formats command.

System Components: Schematic Support

4778	The 64 bit version of SIMetrix 6.0 now works with Altium Designer.

System Components: Schematic System

6122	In Preferences > Schematic > Grids and Units, "Presets" has been renamed to "Altium Presets" to make it clear that user changes made are not saved into the Altium presets. View BugCrunch report #1094.
6180	An intermittent access violation during schematic paste operations when panning has been fixed.

Data Management Packages: Publisher - BoxNet

4488	Users connecting to the Internet via a Proxy Server will now be able to get full access to all content stored in all of our Vaults & also any Vault they set-up & is cloud based. This will include downloading, uploading items, getting previews etc.

Data Management Packages: Publisher - FTP

4488	Users connecting to the Internet via a Proxy Server will now be able to get full access to all content stored in all of our Vaults & also any Vault they set-up & is cloud based. This will include downloading, uploading items, getting previews etc.

Data Management Packages: Publisher - S3

4488	Users connecting to the Internet via a Proxy Server will now be able to get full access to all content stored in all of our Vaults & also any Vault they set-up & is cloud based. This will include downloading, uploading items, getting previews etc.

Data Management Packages: Version Control - SVN

5678	Support for Subversion 1.7 added, including support for the new working folder format as well as updating the built-in Subversion Client to version 1.7.4. View BugCrunch report #838.

Embedded Design Tools: Software Platform

6154	Fixed calculation error in posix_timespec_subtract() and compiler warning in posix_valid_timespec().
6156	Very small timeout values on POSIX mq_timedreceive() no longer result in lost timeout event and waiting forever.

Importers and Exporters: Exporter - Hyperlynx

6078	PCB Save As Hyperlynx now exports POLYGON and POLYVOID coordinates to a precision level that is more acceptable to Hyperlynx readers.

Importers and Exporters: Importer - Accel

5604	P-CAD's polygon shaped component pads and their net assignments are now accurately reflected when importing PCB designs.
6123	PCB P-CAD Import - PCB Library import now creates objects that are mapped to mechanical layers numbered 17 and above using a proper (0, 0) origin, not (-50,000, -50,000) mils. View BugCrunch report #799.

Output Generators: Output - Gerber

6121	Drill Drawing, Drill Guide Layers objects are not exported to Gerber for mirrored Embedded Board Arrays. View BugCrunch report #745.

Output Generators: Output - ODB

6132	ODB++ custom symbols will again be generated as required when the design uses fills rotated at non-orthogonal angles & the ODB++ data will correctly load into any of the Valor tools & other 3rd party applications that load ODB++. View BugCrunch report #1480.

Development updating various modules

The development made for the following tickets required changes to our Run Time Libraries, and as a result require majority of the modules to be updated.

4488	Users connecting to the Internet via a Proxy Server will now be able to get full access to all content stored in all of our Vaults & also any Vault they set-up & is cloud based. This will include downloading, uploading items, getting previews etc.
4778	The 64 bit version of SIMetrix 6.0 now works with Altium Designer.
6127	It is now possible to add parameters to Projects and Project Variants through scripts. View BugCrunch report #1085.

Altium Designer Update 20 (Platform Build 10.1133.24352) – Jun 21, 2012

Key highlights

New PCB connection drawing options

New options have been implemented in the “View Configurations” dialog for "Show All Connections In Single Layer Mode" and "Use Layer Colors For Connection Drawing". For further details, read *Altium Wiki*. View *BugCrunch report #1034* and *BugCrunch report #1035*.

Support for Lattice Diamond

Lattice Diamond software is now supported in Altium Designer for designs targeting Lattice FPGAs. In addition, Lattice iostandard constraints have been improved and are correctly mapped.

Further improvements to 3D Mechanical CAD interfaces in PCB

Improvements include a change in the STEP file output to use the "Component Suffix" option for the Board Part, and a warning has been added to the PCB IDF Export utility for when it detects an empty component comment. *View BugCrunch report #1200.*

Support for alternate PDF readers

Altium Designer will now utilize the default PDF reader for the system, regardless of whether Adobe Reader is installed. View *BugCrunch report #1346*.

System Components: Altium Designer Base

6243	ComboBox value will be committed before scrolling or resizing the "Find Similar Objects" dialog. *View BugCrunch report #928*.

System Components: Altium Designer Installation System

6209	Model previews no longer show a 403 Forbidden error in Vault Explorer.

System Components: Altium Designer Localization

6190	Updated Japanese localization of Altium Designer.
6191	Updated Simplified Chinese localization of Altium Designer.

System Components: Data Management

6209	Model previews no longer show a 403 Forbidden error in Vault Explorer.
6226	Improved Component Release Manager so that leading or trailing white space does not cause a Duplicate item revision parameter HRID error when releasing a component.

System Components: PCB System

6186	The PCB Compare and Merge Panel now detects pad and via hole size differences in the same manner in which it detects pad/via size and shape differences. View BugCrunch report #1237.
6188	PCB Editor's Object Class Explorer now includes shelved polygons when presenting contents of polygon classes. View BugCrunch report #1576.
6189	Implemented new drawing options "Show All Connections In Single Layer Mode" as well as "Use Layer Colors For Connection Drawing". These options can be found in "View Configurations dialog" ("Board layers and colors") on the "View Options" tab. Read Wiki information. View BugCrunch report #1034. View BugCrunch report #1035.
6279	Added forward compatibility warning for Air Gap attribute in Polygon Connect style rule when loading older PCB documents.

System Components: Schematic System

4044	The Sch:ChangeCurrentTemplate command has been fixed so that it can again be run via a script without additional special parameters specified.
6176	Fixed an issue where the right-click menu did not show the option to place a No ERC for some types of violations.
6213	An issue with caching of bitmaps when pasting into schematics has been fixed.
6218	The schematic Document Options dialog box is now resizable. View BugCrunch report #122.

System Components: Soft Design System

2381	Lattice Diamond toolchain is now supported.
4979	Previously, when creating a core component failed for Lattice FPGAs the .edn files of the sub components were missing. This issue is fixed.
5739	Lattice pad file import has been improved. When non-Lattice io standard is used in FPGA design, Altium Designer will issue a warning in the messages panel.
5798	Port names used in Altium Constraint files are automatically converted to upper cases in generated vendor constraint files. View BugCrunch report #1247.

FPGA Design Tools: Ancillary VHDL Synthesis Libraries

2381	Lattice Diamond toolchain is now supported.

Importers and Exporters: Exporter - IDF

6192	PCB IDF Export utility now produces a warning when it detects an empty component comment (this field is required for purposes of setting IDF library file Part Number).

Output Generators: Output - STEP

5903	The STEP file output has been changed to use the "Component Suffix" option for the Board Part in the STEP file output. View BugCrunch report #1200.

PCB Design Tools: PCB Configurable - Atmel QTouch

6244	The Atmel QTouch.IntLib is no longer missing in the Library directory after installing the Atmel QTouch plug-in.

Development updating various modules

The development made for the following tickets required changes to our Run Time Libraries, and as a result require majority of the modules to be updated.

2381	Lattice Diamond toolchain is now supported.
5737	Lattice pad file import has been improved. Port names with '_' in names are correctly handled with differential io standards.
5798	Port names used in Altium Constraint files are automatically converted to upper cases in generated vendor constraint files. View BugCrunch report #1247.
5880	Fixed a bug where the default PDF reader was ignored if Adobe Reader had been installed. View BugCrunch report #1346.
6209	Model previews no longer show a 403 Forbidden error in Vault Explorer.
6212	Fixed crash when project search path contained files larger than 2GB.
6226	Improved Component Release Manager so that leading or trailing white space does not cause a Duplicate item revision parameter HRID error when releasing a component.
6243	ComboBox value will be committed before scrolling or resizing the "Find Similar Objects" dialog. View BugCrunch report #928.

Altium Designer Update 21 (Platform Build 10.1181.24817) – July 24, 2012

Key highlights

Improvements to Re-Annotate

Re-annotate has been improved and now includes options for what to re-annotate (top & bottom, top only, bottom only, selected), and optionally allows for the protection of component with locked designators. Another new option is a user-definable location tolerance (Comparison Threshold), which allows components that are slightly out of line to still be annotated in a logical manner. Re-annotate now also uses the component bounding rectangle (without designator), where it previously used the bounding rectangle that included the designator, which could result in undesirable annotation results. View Wiki info. View BugCrunch report #1453.

Auto-Zoom in Cross Select Mode

Auto-zooming in Cross Select Mode has been enabled, with three options available: No Zoom, Zoom to Last Selected, and Zoom to All. View Wiki info. View BugCrunch report #1468.

Updated support for vendor tools

Xilinx ISE v14.1 and Altera QuartusII v11.1 and v12.0 are now supported.

System Components: Altium Designer Base

6252	Fixed a crash that occurred on some designs after compiling the document once.
6301	Fixed incorrect order of section selection entries in automatically generated LSL file.
6306	New auto-zooming options added for Cross Select Mode (No Zoom, Zoom to Last Selected and Zoom to All). View Wiki info. View BugCrunch report #1468.
6323	DBLib performance has been significantly improved when using Oracle datasources by querying only the tables for the SCHEMA selected by the user.
6351	Variants now correctly support parameter variations for a New Value set to blank where the Original Value contains a value. View BugCrunch report #983.
6355	Added an option in the "PCB Printout Properties" dialog to choose the data to display in component designator. View BugCrunch report #153.
6356	A progress GUI in the VCS Command Dialog is provided to indicate the current progress in a time consuming process. The process can be terminated by clicking the Cancel button. View BugCrunch report #1060.

System Components: Altium Designer Localization

6308	Japanese localization of Altium Designer has been updated.
6309	Simplified Chinese localization of Altium Designer has been updated.

System Components: PCB System

2656	Re-annotate now allows for option of what to re-annotate (top/bottom, top only, selected, etc) and optionally allows to protect components with locked designators. View Wiki info. View BugCrunch report #772.
3428	Re-annotate no longer uses the designator location for ordering the components - component bounding rectangle is used instead. New optional user-defined tolerance (Comparison Threshold) can be utilized to allow components that are slightly out of line to be annotated in logical manner. View Wiki info. View BugCrunch report #1453.
5869	Fixed Interactive Diff Pair Router to change gap on layer change to match rule. View BugCrunch report #1092.
6225	DRC now properly detects disconnected stacked blind/buried vias when smart track ends option is used. View BugCrunch report #1859.

6296	Fixed application hang caused by erasing entry in the MaxVias design rule. View BugCrunch report #1525.
6306	New auto-zooming options added for Cross Select Mode (No Zoom, Zoom to Last Selected and Zoom to All). View Wiki info. View BugCrunch report #1468.
6317	Fixed PCB crash when component is located outside of PCB workspace.

System Components: Schematic System

6282	User can start a new search from the "Find Text - Jump" directly. View BugCrunch report #1441.
6306	New auto-zooming options added for Cross Select Mode (No Zoom, Zoom to Last Selected and Zoom to All). View Wiki info. View BugCrunch report #1468.
6350	Schematic wire mode will now remain in 45 Degree mode or Auto Wire mode when connecting to a hotspot, rather than always switching to 90 Degree mode. View BugCrunch report #1055.
6351	Variants now correctly support parameter variations for a New Value set to blank where the Original Value contains a value. View BugCrunch report #983.

System Components: Soft Design System

6165	Xilinx ISE versions up to 14.1 included are now supported.
6283	Altera QuartusII v11.1 and v12.0 are now supported.

Hardware Support Packages: Device Support - Lattice XP

6173	The right mouse click Program Flash With Current Project command in the Devices View is now working as expected when launched from a Lattice XP device.

Importers and Exporters: Exporter - IDF

1859	An issue has been corrected in the IDF Exporter whereby components would be placed below the top surface. View BugCrunch report #1847.
6187	Changed IDF Export/Import to use the PCB Board. View BugCrunch report #513.

Importers and Exporters: Importer - IDF

6187	Changed IDF Export/Import to use the PCB Board. View BugCrunch report #513.

Output Generators: Output - Gerber

6339	Now the Gerber Paste Mask generation is correct when Flipped Embedded Board Arrays are used with PCBs containing custom polygon region paste mask shapes placed on the Paste layer.

Output Generators: Printer - PCB

6304	PCB Variant Text for "not fitted" parts is no longer reversed in printouts. View BugCrunch report #246.
6355	Added an option in the "PCB Printout Properties" dialog to choose the data to display in component designator. View BugCrunch report #153.

Development updating various modules

The development made for the following tickets required changes to our Run Time Libraries, and as a result require majority of the modules to be updated.

6286	Spansion S29GLXXXA/M/N in system flash programming no longer fails when Nios II processor is used.
6306	New auto-zooming options added for Cross Select Mode (No Zoom, Zoom to Last Selected and Zoom to All). View Wiki info. View BugCrunch report #1468.
6351	Variants now correctly support parameter variations for a New Value set to blank where the Original Value contains a value. View BugCrunch report #983.
6355	Added an option in the "PCB Printout Properties" dialog to choose the data to display in component designator. View BugCrunch report #153.

Altium Designer Update 22 (Platform Build 10.1271.26245) – October 19, 2012

Key highlights

Delete selected objects
We have included a new feature in PCB Editor for deleting of selected objects (through the shortcut keys Ctrl+Delete), which then selects adjacent routed objects for further unrouting. When single end-of-route object is selected, Backspace shortcut now deletes selection and auto-selects connected singular route object. Each of these shortcuts can be used in a successive manner to incrementally unwind routed paths. View BugCrunch report #916. View wiki info.

New module for output of IDF
This release has the addition of a new plugin “Output - IDF” found in the Output Generators category. This new plugin provides IDF export capability in the OutJob “Export Outputs” section. View BugCrunch report #1363. View wiki info.

Updated FPGA device and vendor tools support
Xilinx ISE v14.2 and Lattice Diamond 2.0 are now supported.
Ultra and micro fineline ball grid array (UBGA & MBGA) devices have been added to the Altera Cyclone4E Nexus driver.

System Components: Altium Designer Base

6366	Give a better file name of each library report image while creating a browser style library report. View BugCrunch report #1560.
6397	Footprints included by PCBLib but not by DBLib can now be found. View BugCrunch report #1506.
6416	Net class directives attached to Blanket objects no longer produce incorrect "Duplicate Net Names Wire N000-1 (inferred)" compiler messages. View BugCrunch report #1944.

System Components: Altium Designer Localization

6204	Traditional Chinese localization of Altium Designer has been updated.
6387	Japanese localization of Altium Designer has been updated.
6388	Simplified Chinese localization of Altium Designer has been updated.

System Components: PCB System

5922	The interactive router option Allow Diagonal Pad Exits now works correctly for surface mount pads.

6373	PCB Tools >> Reannotate now allows the start index to be set.
6413	Fixed Interactive Diff-Pair router crash that would cause PCB to hang.
5504	Fixed slow response/hang when dragging a track near very large keepout arcs.
6494	Fixed problem with Copy Room Formats that would cause tracks in the room to not have their net assignment updated correctly after the copy.
6527	Fixed bug in Copy Room Format where vias sometimes would not be copied.
6432	PCB Editor Ctrl+Delete shortcut now deletes selection and auto-selects all route objects connected to deleted ones. When single end-of-route object is selected, Backspace shortcut now deletes selection and auto-selects connected singular route object. View BugCrunch report #916.

System Components: Schematic Support

6406	Internal memory options for FPGA LAX have been extended to support 8K, 16K, 32K and 64K entries. View BugCrunch report #1457.

System Components: Schematic System

6360	Place full circle is now available in Schematic: Place >> Drawing Tools >> Full Circle. View BugCrunch report #1050.
6391	Images in schematic document can be rotated now.

System Components: Soft Design Support

6406	Internal memory options for FPGA LAX have been extended to support 8K, 16K, 32K and 64K entries. View BugCrunch report #1457.

System Components: Soft Design System

6407	Lattice Diamond version 2.0 is now supported.
6403	Xilinx ISE 14.2 is now supported.
6374	Ultra and micro fineline ball grid array (UBGA & MBGA) devices have been added to the Altera Cyclone4E Nexus driver.

System Components: Cyclone4E

6374	Ultra and micro fineline ball grid array (UBGA & MBGA) devices have been added to the Altera Cyclone4E Nexus driver.

FPGA Components: Instrument - Logic Analyser

6406	Internal memory options for FPGA LAX have been extended to support 8K, 16K, 32K and 64K entries. View BugCrunch report #1457.

Importers and Exporters: Exporter - IDF

6379	IDF Export is now handling the units and the board origin offset correctly. View BugCrunch report #513.

Importers and Exporters: Importer - IDF

6379	IDF Export is now handling the units and the board origin offset correctly. View BugCrunch report #513.

Importers and Exporters: Importer - Allegro

5716	Allegro Importer into PcbDoc now detects objects of Class "Constraint Region" and imports them as Mechanical 1 layer outlines.

Output Generators: Output - AdvSim

6406	Internal memory options for FPGA LAX have been extended to support 8K, 16K, 32K and 64K entries. View BugCrunch report #1457.

Output Generators: Output - Gerber

6405	Gerber flashes are now created correctly for solder/paste mask features created automatically (from solder/mask expansion properties) for fills, tracks and arcs when mirrored Embedded Board Arrays are used.

Output Generators: Output - IDF (New Module)

6385	Added a new module "Output - IDF' to supply IDF Exporter capability in the OutJob "Export Outputs" section. View BugCrunch report #1363.

Development updating various modules

The development made for the following tickets required changes to our Run Time Libraries, and as a result require majority of the modules to be updated.

6281	Auto-increment will now increment trailing numbers that are preceded by a period "." or hyphen "-" for Smart Paste, shift-duplication, designators while placing parts, pins, components, pads, and for SchLib Component Rule Check. View BugCrunch report #1503.
6406	Internal memory options for FPGA LAX have been extended to support 8K, 16K, 32K and 64K entries. View BugCrunch report #1457.
4583	A run-time error (wbtc.exe) dialog no longer pops up during the build flow while multiple versions of Xilinx ISE have been installed on the same computer.

Altium Designer Update 23 (Platform Build 10.1327.26514) – November 19, 2012

Key highlights

New deselect touching line and rectangle commands

The PCB editor and PCB library editor have been updated with new commands to deselect objects by touching rectangle or touching line.

Easier polygon pour order management

You can now modify the polygon pour order within the Polygon Manager (Tools>>Polygon Pours>>Polygon Manager) by using drag and drop. This can greatly speed up the reordering process when dealing with a large amount of polygons. View wiki info.

PCB Rule dialog improvements

New options have been added to the PCB Rules and Constraints Editor dialog (Design>>Rules) allowing you to delete multiple selected rules. View BugCrunch report #1136. View wiki info.

Importer improvements

This update includes additional improvements to the Mentor PADS PCB, PADS Logic and Expedition importers.

Updated support for vendor tools and devices

Xilinx ISE v14.3, Lattice Diamond 2.0.1, Altera QuartusII and NiosII version 12.0 SP2 are now supported. Software Platform support for Atmel AT86RF231 Wireless 802.15.4 device is now available - including LR-WPAN physical layer with generic AES encryption/decryption service. View wiki info.

System Components: PCB System

6587	Altium Designer correctly synchronizes pcb and fpga projects that include Xilinx Spartan 6 devices. View BugCrunch report #1312.
6556	Fixed freeze/slowness when activating the route tool or initiating a drag track edit. View BugCrunch report #2122.
6254	Allow Drag/Drop in Polygon Manager Pour order.
6498	Fixed Loop Remove issue when the finished route barely touches a pad, causing incorrect tracks to get removed. View BugCrunch report #1751.
6577	Region handles are now scaled correctly: after the regions have been scaled and a region is selected, the handles of the region appears at the correct locations. View BugCrunch report #639.
6578	Select touching line and rectangle have been fixed and now work for polygon cutouts.
6579	Handling drawing of Arc primitives in region Shape for rooms has been added. View BugCrunch report #1409.
6580	Option to delete multiple rules has been added to Rules dialog. View BugCrunch report #1136.
6581	Commands to deselect touching line and rectangle have been added.

System Components: Soft Design Support

6536	Fixed problem where C code typedef struct editing could freeze Altium Designer.

System Components: Soft Design System

6590	Xilinx ISE version 14.3 is now supported.
6589	Altera QuartusII and NiosII version 12.0 SP2 are now supported.
6591	Lattice Diamond version 2.0.1 is now supported.

Importers and Exporters: Importer - Expedition

6476	Expedition footprint library import - When a library file contains files locations that have unix-style directory delimiters, they are now augmented to conform to Windows-standard paths so that files can be properly found.

Importers and Exporters: Importer - PADS

6507	PADS Import - Use of PADS alphanumeric pin names and pin designators has been corrected to properly set Altium Designer component/footprint pin names and pin numbers.
5093	PADS Import - When importing PCB Layout files, Geometry.Height attributes are now used to set component Height properties.
5549	Pads Import - PADS Logic designs of format V2007.0 and later that contain hierarchical blocks are now successfully imported.
5720	PADS PCB Design Import - Use of PADS clearance rules to create Altium Designer clearance rules has been improved. General categorical rules (such as net clearance rules) use more appropriate clearance values.
6021	PADS Schematic Library Import - PADSLogic library parts that contain zero gates no longer cause empty library file results.
6544	PADS Schematic Library Import - When a custom PADSLogic pin decal reference is not found, the default "PIN" pin decal is used, and a warning is written to the import log file.
6545	PADS Import - PADLogic decal circle pieces are now more reliably imported.

Output Generators: Output - Gerber

6560	Gerber flashes are now created correctly for solder/paste mask features created automatically (via solder/mask expansion properties) for Regions when mirrored Embedded Board Arrays are used.

Output Generators: Output - ODB

6561	ODB++ data are now created correctly for solder/paste mask features created automatically (via solder/mask expansion properties) for regions, fills, tracks & arcs when mirrored Embedded Board Arrays are used.

Embedded Design Tools: TASKING Core

5576	Embedded make utility does not wait for all commands to be finished.

Embedded Design Tools: TASKING CHC

6311	Fixed incorrect issuing of "E489: too many bits stored".
4776	CHC C-library calls are functional again.
5850	The CHC compiler issued an "internal consistency check" if the source file contains a loop with an emty basic block. This is fixed now.

Embedded Design Tools: Software platform

6540	AGUI service now correctly deals with multiple instances in a multi-threaded application.
4657	Several minor bug fixes in the Software Platform graphics service.
4653	Input in Soft Terminal as been improved and is no longer blocking in some situation where the reading buffer is very small.
6574	Software Platform support for Atmel AT86RF231 Wireless 802.15.4 device is now available - including LR-WPAN physical layer with generic AES encryption/decryption service.

Hardware Support Packages: Device Support - Xilinx CoolRunner 2

6532	Generating a programming file for Xilinx CoolRunner 2 devices with QF32 package is now working as expected.

Altium Designer Update 24 (Platform Build 10.1377.27009) – December 18, 2012

Key highlights

Support for Cortex-M3 Discrete Processors
NXP LPC1000 series, STMicroelectronics STM32 and Texas Instruments Stellaris Cortex-M3 devices are now supported.

Support for SEGGER J-Link
Debugger support for SEGGER J-Link debug probe for ARM processors is now available.

FPGA Device Support
Altera Arria2GX FPGAs is now available.

Software Platform Enhancements
This update now includes HTTP client, HTTP server and JSON services in addition to enhancements in the Tasking toolchains.

System Components: PCB System

311	Signal layer keepout tracks are now displayed correctly when keepout layer is turned off. View BugCrunch report #2045.
319	Fixed crash that would occur during loop remove of interactive routing.
351	Duplicating a rule now correctly assigns a new unique ID.
382	Fixed polygon pour manager drag/drop pour order to be properly retained after closing dialog.

System Components: Altium Designer Localization

384	Edit>>Deselect>>Touching Rectangle and Line now appear correctly in localized menus.

System Components: Soft Design Support

18	Flash programming now supports CFI compatible Flash (on TSK3000).
248	Added support for Altera Arria2GX.

System Components: Soft Design System

248	Added support for Altera Arria2GX.
257	Support for DT05 (currently in production), the new generation USB JTAG adapter, based around chip solution from FTDI.
259	Clock frequency constraints are correctly passed on to Lattice PAR tools when Synplify for Lattice is used for synthesis.

Importers and Exporters: Importer - PADS

378	PADS Import - Processing of schematic library part types has been corrected for connectors that have pin definitions, but indicate zero gates.

Importers and Exporters: Exporter - Hyperlynx

357	When a PCB design containing a split plane comprised of more than 5000 boundary segments was saved in Hyperlynx format, an unexpected condition could occur.PCB designs with large/complex split planes are successfully saved in HyperLynx format.

Output Generators: Output - ODB

308	True Type text on mechanical layers can now be correctly added to all plots in ODB++ output. View BugCrunch report #1514.
309	Regions and fills placed directly on solder and paste layers and output to ODB++ via a flipped embedded board now behave correctly. View BugCrunch report #1760. View BugCrunch report #2041.

Embedded Design Tools: Software platform

227	Endianness macros in util_endian.h have been fixed.
232	Software Platform function netif_ethernet_stop() does not cleanup DHCP resources.
234	Compilation errors in drv_emac32_internal.c if wait modes in Software Platform EMAC32 Driver are set to Notify.
237	EMAC32 driver now correctly supports link status call back.
238	Software Platform should allow setting link status callback before starting the network layer.
239	Software Platform now includes HTTP client and HTTP server services.
240	Software Platform now includes JSON parser service.
249	Software Platform document: setting EMAC32 PHY address moved from peripheral to driver.
251	Software Platform socket functions now set errno value on error.
252	The remaining time value that is returned by nanosleep after it has been interrupted by a signal is now correct.

Embedded Design Tools: TASKING TSK3000

225	Assembler sometimes creates a illegal dependency file.
229	Embedded project path may now contain dollar signs ($).
230	Interrupt function in C++ module no longer leads to compilation errors.
236	Custom LSL files can now include generated project LSL files.
244	Debugger emits "Unknown name" message for single character variable name.
250	Wrong optimization by TSK3000 compiler in some scenarios involving a volatile variable.
255	Debugger can now find project source files if executable is built externally.

Embedded Design Tools: TASKING ARM

225	Assembler sometimes creates a illegal dependency file.
229	Embedded project path may now contain dollar signs ($).
230	Interrupt function in C++ module no longer leads to compilation errors.
236	Custom LSL files can now include generated project LSL files.
244	Debugger emits "Unknown name" message for single character variable name.
255	Debugger can now find project source files if executable is built externally.

Embedded Design Tools: TASKING MicroBlaze

225	Assembler sometimes creates a illegal dependency file.
229	Embedded project path may now contain dollar signs ($).
230	Interrupt function in C++ module no longer leads to compilation errors.

236	Custom LSL files can now include generated project LSL files.
244	Debugger emits "Unknown name" message for single character variable name.
255	Debugger can now find project source files if executable is built externally.

Embedded Design Tools: TASKING Niosll

225	Assembler sometimes creates a illegal dependency file.
229	Embedded project path may now contain dollar signs ($).
230	Interrupt function in C++ module no longer leads to compilation errors.
236	Custom LSL files can now include generated project LSL files.
244	Debugger emits "Unknown name" message for single character variable name.
254	Nios ERET instruction encoding not properly simulated or disassembled.
255	Debugger can now find project source files if executable is built externally.

Embedded Design Tools: TASKING PowerPC

225	Assembler sometimes creates a illegal dependency file.
229	Embedded project path may now contain dollar signs ($).
230	Interrupt function in C++ module no longer leads to compilation errors.
236	Custom LSL files can now include generated project LSL files.
244	Debugger emits "Unknown name" message for single character variable name.
255	Debugger can now find project source files if executable is built externally.

Embedded Design Tools: TASKING Core

229	Embedded project path may now contain dollar signs ($).
230	Interrupt function in C++ module no longer leads to compilation errors.

Embedded Design Tools: TASKING 8051

236	Custom LSL files can now include generated project LSL files.

Embedded Design Tools: TASKING TSK165x

236	Custom LSL files can now include generated project LSL files.

Embedded Design Tools: TASKING Z80

236	Custom LSL files can now include generated project LSL files.

Hardware Support Packages: Device Support - NXP LPC1000

243	Compiler, debugger and Flash programming support for various Cortex-M3 devices.

Hardware Support Packages: Device Support - STMicroelectronics STM32

243	Compiler, debugger and Flash programming support for various Cortex-M3 devices.

Hardware Support Packages: Device Support - Texas Instruments Stellaris

243	Compiler, debugger and Flash programming support for various Cortex-M3 devices.

Hardware Support Packages: Device Support - SEGGER J-Link

246	Debugger support for SEGGER J-Link debug probe for ARM processors.

Hardware Support Packages: Device Support - Altera Arria II GX

248	Added support for Altera Arria2GX.